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Power-pulsing of the CMOS sensor Mimosa 5

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Abstract

In order to meet the stringent requirements for vertex detectors at the ILC the average power consumption of the detector has to be reduced as far as possible. Turning-off the power for the time between the bunch trains is one possibility. This note describes the performance of the CMOS sensor Mimosa 5 under power-pulsing conditions. The study shows that about 0.9 ms are needed before data taking to turn on the power in order to reach close to stable performance. But it needs about 5 ms to reach the full performance of constant-power conditions.

1 Introduction

The extreme requests to vertex detectors at the ILC require a very low material budget for penetrating particles. This leads to sensors possibly thinned down to below 50 μm, extremely light support which nevertheless is very stable, minimum in cabling and a minimum of material for cooling. The goal for cooling is to use cooling by cold gas at moderate flow rates to avoid vibrations. But this cooling cannot cope with the DC power being used for current sensors which would add up to about 500 W and more for a full vertex detector. However the beam structure of the proposed linac which will run with trains of about 1 ms length and a train rate of 5 Hz provides the ability to save power by turning on the devices within the vertex detector for as little as 1 ms thus saving power by a ratio of approx 1/200 at best.

2 The Mimosa 5 sensor and its readout

We have studied the performance under power-pulsing conditions of the large Mimosa 5 chip (approx 400 mm^2) which has been used extensively over the last years for general performance studies [Ref.1]. This sensor will definitely not be the sensor which will be used for the final vertex detector. But it is the largest CMOS sensor available right now, has been studied extensively, and is embedded in a readout infrastructure which can be modified easily. In addition the current supply for the output buffer-amplifier has been brought out to an external bond pad. This allows an independent treatment of the power for the most current consuming part of the sensor. We have measured the pedestal and noise performance under the influence of power-pulsing. Also the collection of charge from interacting photons of a ^{55}Fe source has been studied. The sensors, the auxiliary and the imager boards together with the readout infrastructure have been provided by IreS/Strasbourg.

The Mimosa 5 sensor consists of 4 matrices of 256k pixel each organized in a 512 by 512 matrix. The pixels have a pitch of 17 μm. The 4 matrices are read out via 4 output buffers (Fig.1).

The output buffers consume up to 15 mA, the remaining analog and digital part only about 1 mA, each. The power is provided to the sensor via bond pads for digital, analog and buffer power. This allows an easy modification of the readout infrastructure which then provides the possibility to switch the output buffer part on and off independently from the rest of the sensor which is kept under power. So about 15 mA of the total 17 mA can be turned on and off by a special switch which is controlled by the sequence of the readout signals of the Mimosa 5, so 88% of the power consumption can be turned on and off.

The readout infrastructure of the Mimosa 5 sensor consists of a VME unit, the imager card for digitizing and controlling the readout with two FPGAs. This board sends out the clock signal and other control signals to an auxiliary board which transmits the signals together with power to the sensor board. The sensor board sends the analog signals, buffered by discrete amplifiers, to the auxiliary board from where they are sent after another buffering to the FADCs of the imager card for digitisation. The power for the sensor board

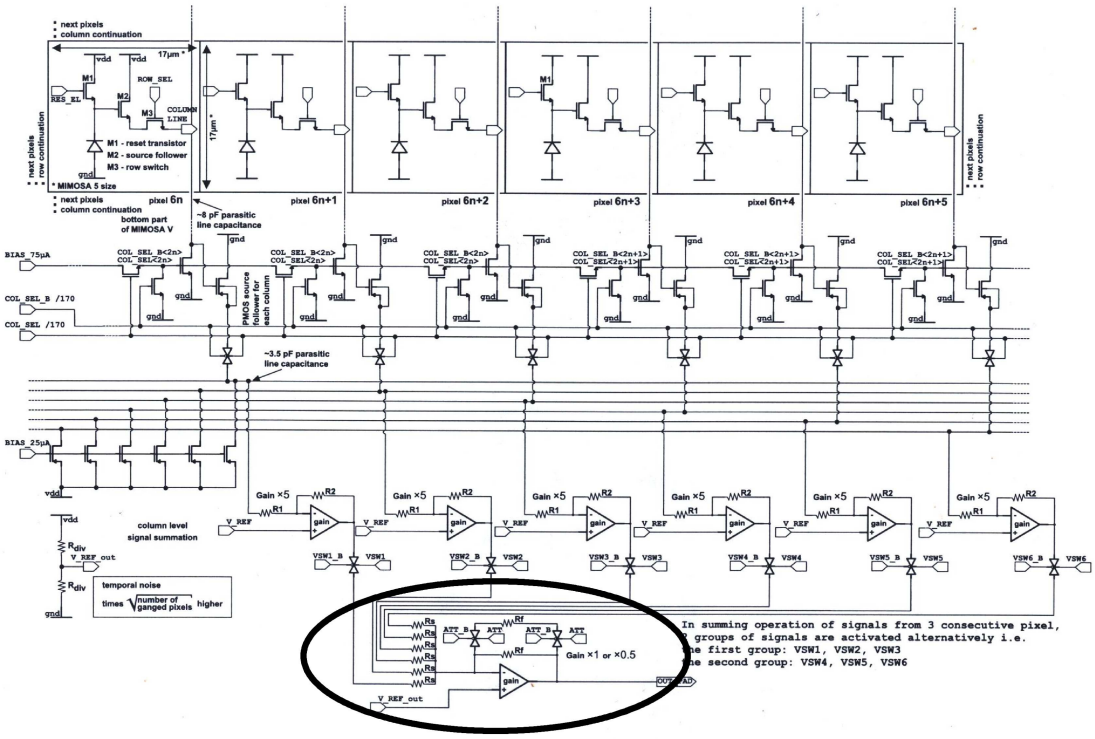


Figure 1: Schematics of a matrix of Mimosa 5 readout architecture
The opamp for which the power is pulsed is encircled

is derived via a 5 V voltage regulator from the 10 V power-line. The power distribution after the voltage regulator on the auxiliary board has been modified such that the power line for output buffers is independent from the rest of the sensor. The switch is positioned after this separation. It consists mainly of a MOSFET switch, IRF7455 [Ref.2], with a R_{on} of approx 7 mΩ. This switch is turned on and off controlled by a variable delayed signal which originates from the reset signal of the sensor readout. (Fig.2).

The sensor is read out sequentially with a 10 MHz clock. So a matrix will be read out within 25.6 ms. The readout in double sampling mode starts with a reset signal which is sent simultaneously to one column of each submatrix and continues for 25.6 μs until all charge collecting nodes of the pixels are reset. Then the readout starts and the submatrix is read out an even number of times. Only the last 2 frames of the submatrix are stored in the local memory of the readout card. These data of the 2 frames are then sent, controlled by a program, to the memory of the processor of the VME crate with a speed of 2 MB/sec (size of 1 event 1 MB). This leads to an interruption of about 660 ms before a next readout is started. During this interval the power to the output buffers is turned off. When the processor memory is full the data are sent for permanent storage to a PC hard disk which takes about 4 s (Fig.3). For this study we have chosen to read out the 3^{rd} and

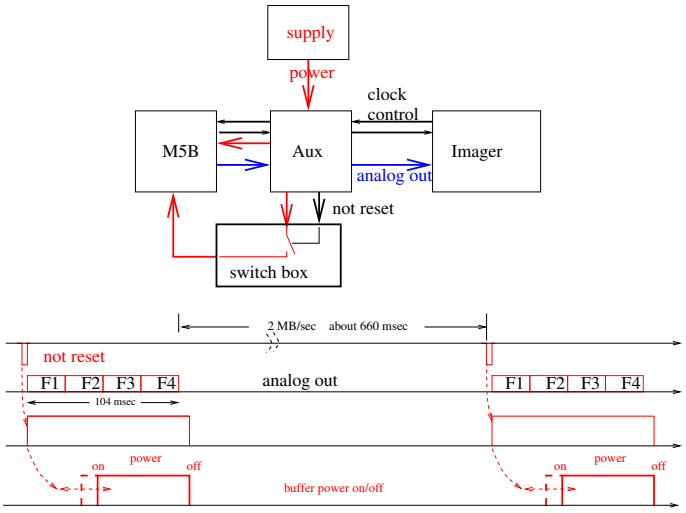
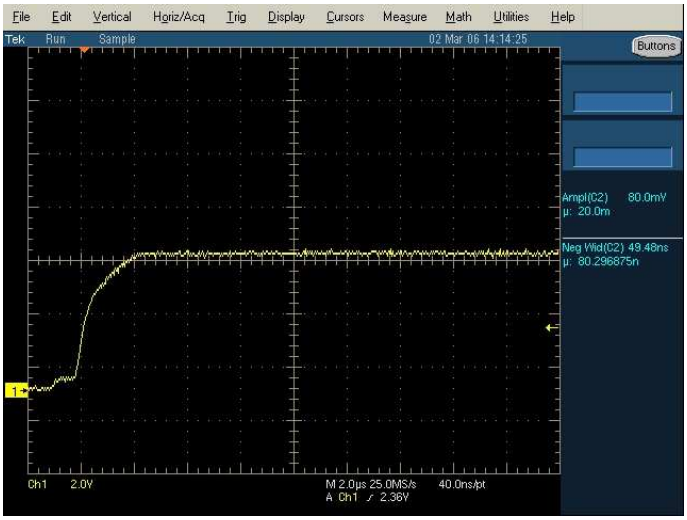


Figure 2: Principle schematics of power-pulsing

the 4^{th} frame and turn on the power during the 2^{nd} frame preceeding the two. The control of the switching is synchronised with the reset signal of the sensor. Even for constant power the 1^{st} and 2^{nd} frame still showed some unexplained strange behaviour, possibly due to the influence of the reset procedure.

3 Performance of power pulsing

The power of 10 V to the setup is provided by an HP power supply which reaches the auxiliary board after a series of capacitors (ceramic and Tantal) and an inductor of 10 μH. After the 5 V voltage regulator which only uses bypass capacitors (ceramics and Tantal) the voltage line is split into the output buffer, the remaining analog and the digital voltage line. These 3 voltages are sent via a short cable to the sensor board. On the sensor board the lines for the digital and remaining analog are received by a series of bypass capacitors together with an inductor in the line. Only the output buffer line is controlled and bypassed by ceramic and Tantal capacitors alone. No inductor is used for the buffer line. The performance of the switch connected to the auxiliary board has been tested with a number of special loads. With the load of 100 Ω to ground leading to 50 mA current to be switched the voltage rises to the final value within approx 3 μs (Fig.3). An additional 47 μF capacitor increases the time to full voltage to approx 300 μs. After switching off, the voltage decreases with an RC time of 4.8 ms. When the sensor board is connected to the switch with an additional 47 μF to ground the time to full voltage increase further to 600 μs.



a: rise-time of power for a resistive load (note 2μs/div)

b: one readout cycle: data and power signal (note 2s/div)

Figure 3: Power-pulsing

4 Results of power-pulsing studies

Fig.4 shows the effect of powerpulsing. The DC level of the output signal during power-off is shifted by about 100 mV above the constant power case. After power-on it approaches the equilibrium with some oscillation despite the fact that the DC power is already stable again. This causes the strong oscillation of the pedestals.

All data discussed from here on are CDS data ('Correlated Double Sampling') which were taken at -10^{o}C. First tests have shown that the 4^{th} frame is not influenced anymore when the power was switched on around the readout start for matrix 3.

We show the effect of pulsing for two turn-on times relative to the row marker from where the readout of the matrix starts:

- 0.34 ms before the row marker, with the power
  still approaching the final value when the readout starts (Fig.4b).
- 1.2 ms after the row marker,
  clearly within the readout time of the frame

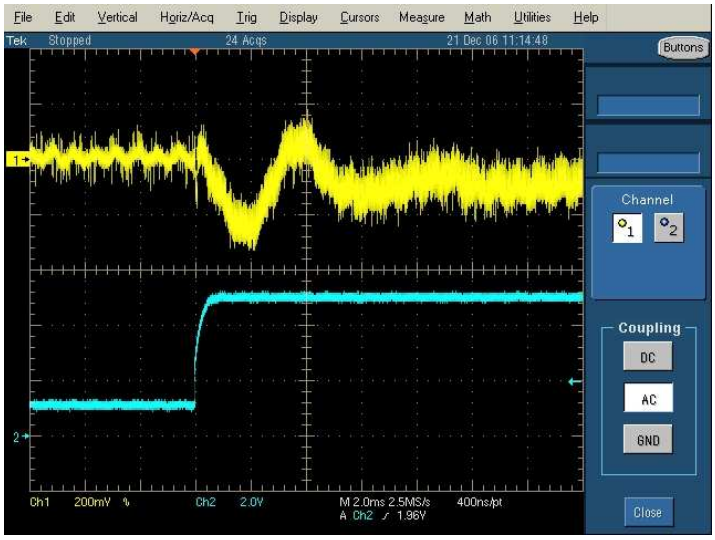
Fig.5 shows the pedestal and noise performance of the full matrix for each individual pixel for 3 different power conditions. The data show the raw data with no selection cut applied for large pedestals and noise or otherwise not well behaving pixels. These bad performing pixels nevertheless add up to only around 1% of the total number of pixels. The average pedestal and noise numbers for constant power (Fig. 5a) are about 6 and 2.8 ADC channels, respectively. This noise number translates into about 29 electrons, good enough to separate the K_α and K_β peaks in the ^{55}Fe spectra clearly.

Fig.5b shows the performance for power-on 0.36 ms before the row marker. After about 0.5 ms the DC voltage has reached the nominal voltage. The pedestal value oscillates and the noise is decreasing. After 0.5 ms after the row marker, 0.86 ms after power-on, the noise has reached a value of smaller or equal 4 ADC channels with some small oscillation of the noise value. Only after 5.4 ms after power-on the noise value reaches the stable value of the constant power case.

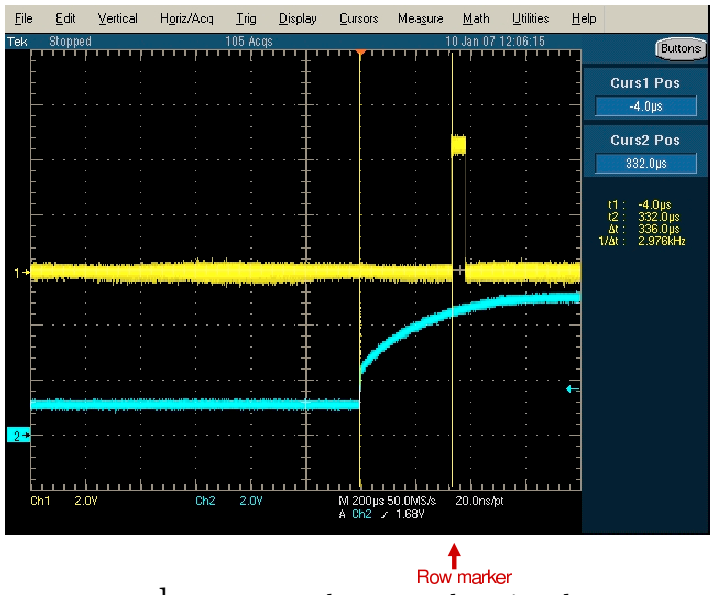
Fig.5c shows the case of power-on 1.2 ms after the row marker. One sees the status of the turned-off output. Then the performance is the same as for the previous case, shifted only by 0.36 + 1.2 ms in time.

The reasons for the pedestal oscillation and the oscillation of the noise by about 1 ADC channel are not understood. It seems that the DC power is not the cause for the pedestal variations, since it has reached at that time already its final value without oscillations and is stable. Possibly only simulations of the sensor readout can give some explanation. The most remarkable result is that pedestals with values oscillating between -400 and +200 ADC counts subtract out in CDS to a noise level close to the constant power noise values.

Fig.6a-c show the results for ^{55}Fe data for the 3 different powering conditions. The figures show the seed pixel noise and the energy spectra fitted to a double Gaussian distribution. The events have been selected after appropriate cuts for bad pixels for a S/N of > 10 for the seed pixel and a S/N < 2 for neighbouring pixels, thus selecting mainly events where the X-rays are converted directly underneath the seed pixel. For the cases of powerpulsing



a: analog output and power signal (2 ms/div)



b: power and row marker signal:
power-on 0.36 ms before row marker (200 μs/div)

Figure 4: Effects of powerpulsing. Note different time scales

the data of the time interval (eg pixel range) were used which starts with that time/pixel number, for which the noise has reached a value of 4 ADC channels, and ends, when the constant noise of the constant power case has been reached again. During this time interval the pedestals are still strongly oscillating.

As expected the noise for the powerpulsing cases (Fig.6b,c) shows a wider distribution with tails towards higher noise values which result in increased values of the mean noise of around 4 channels. But the two ^{55}Fe X-ray lines are still visible with the resolution worsened somewhat. Only if one uses data after the first 5.4 ms after power-on one reaches again the noise and resolution of the constant power case.

5 Conclusion

The measurements show that after 0.9 ms after turn-on of the power of the output buffers of the Mimosa 5 sensor the performance of the sensor has already reached noise values of 4 ADC channels, approaching the constant power case with some small oscillations of the noise, but still with strong variations of the pedestals. Data in the time interval from 0.9 up to 5.4 ms after power-on show a mean noise value of 4 ADC channels corresponding to 40 electrons. Only the data after the first 5.4 ms after power-on show noise values of 3 ADC channels, eg 30 electrons, similar to the constant power case. If the increased noise during the first 5.4 ms after power-on can be tolerated the power dissipated in the output buffer could be reduced by a factor of close to about 200, assuming a 1 ms bunchtrain and a repetition rate of 5 Hz, leaving it negligible compared to the remaining power of about 2 mA used in the digital and the remaining analog part. This reduces the overall power dissipation by a factor of 8 relaxing the requirements for cooling systems. But the full noise performance can be only reached at the expense of a higher power dissipation since the reduction factor decreases to about 40.

Future designs will include the power saving requests and will lead to even higher savings in average power. It remains to be seen how far the chip can be turned off and still avoid reprogramming of the sensors after every bunch train. The reprogramming would of course add to the power budget. The reported result is encouraging because it shows that even a sensor which has not been designed with power pulsing in mind is performing well very soon after power turn-on.

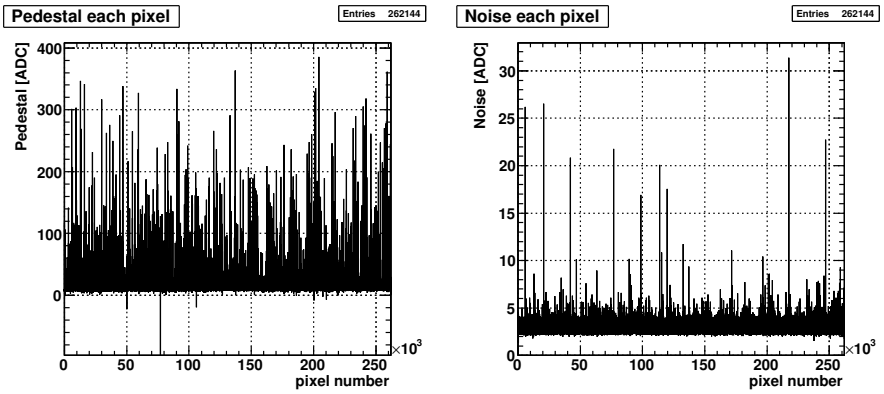
Acknowledgment

We would like to thank our colleagues at IreS/Strasbourg for bringing the problem of power-pulsing to our attention and for providing us with the necessary hard- and software. We thank D. Contarato for introducing us into the MAPS analysis software and T. Klimkovic for her help in the early phase of the study.

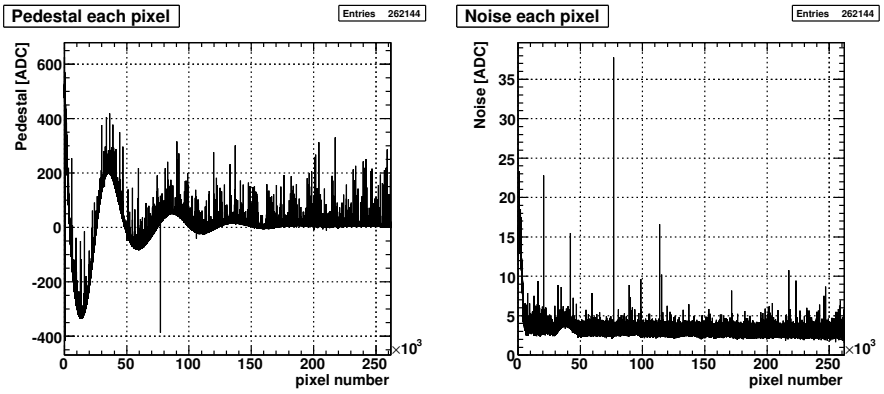
References

[1] G. Deptuch PhD thesis IreS/Strasbourg 2002

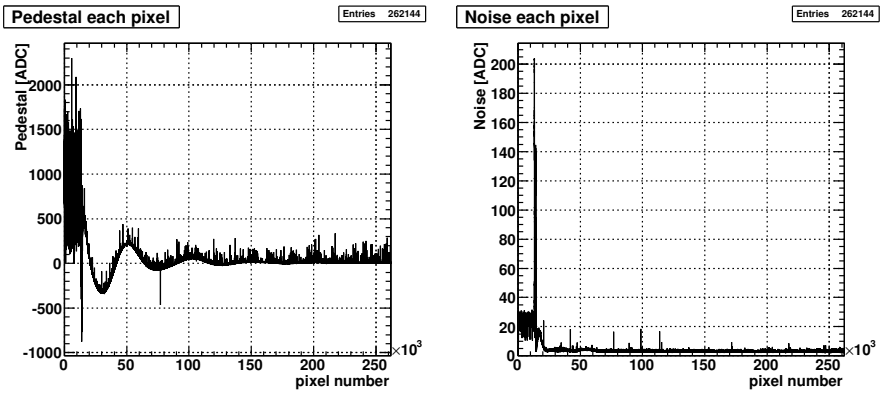
[2] product of International Rectifier



a: constant power

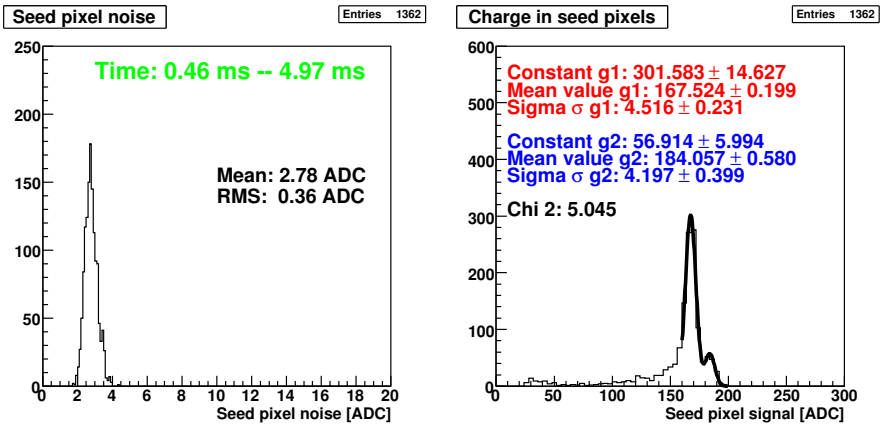


b: power on 0.36 ms before row marker

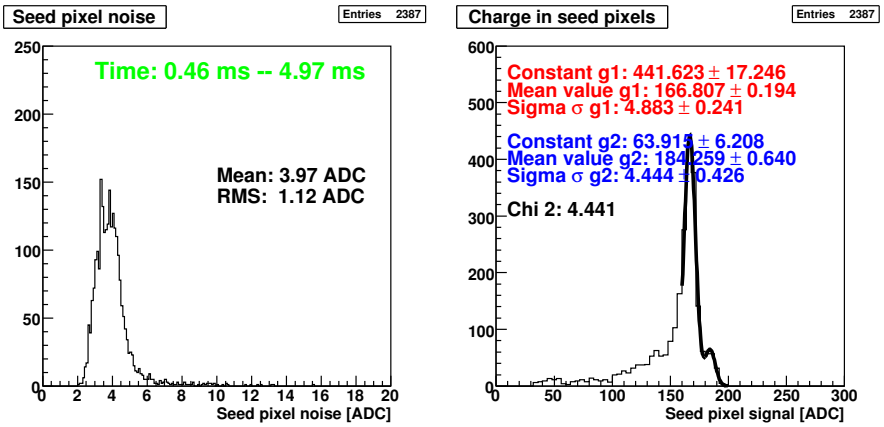


c: power on 1.2 ms after row marker

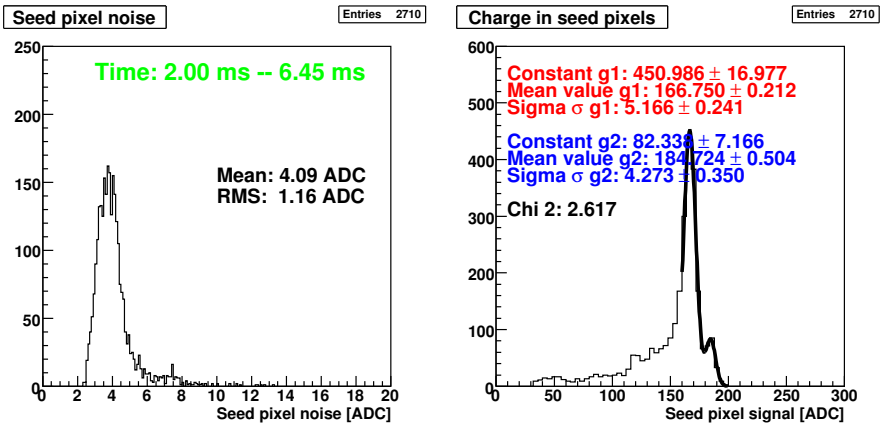
Figure 5: Raw pedestal and noise against pixel number, no selections applied. 50,000 pixels correspond to 5 ms. Note the different vertical scales



a: constant power



b: power on 0.36 ms before row marker



c: power on 1.2 ms after row marker

Figure 6: Seed pixel noise (left) and seed pixel charge (right) distribution