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# Final AIDA report on the development of readout electronics for a TPC, and some future prospects

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**Abstract**

A high resolution TPC is the main option for a central tracking detector at the future International Linear Collider (ILC). It is planned that the MPGD (Micro Pattern Gas Detector) technology will be used for the readout. A Large Prototype TPC at DESY has been used to test the performance of MPGDs in an electron beam of energies up to 6 GeV. The first step in the technology development was to demonstrate that the MPGDs are able to achieve the necessary performance set by the goals of ILC. For this 'proof of principle' phase, the ALTRO front-end electronics from the ALICE TPC was used, modified to adapt to MPGD readout. The proof of principle has been verified and at present further improvement of the MPGD technology is going on, using the same readout electronics. The next step is the 'feasibility phase', which aims at producing front-end electronics comparable in size (few $mm^2$) to the readout pads of the TPC. This development work is based on the succeeding SALTRO16 chip, which combines the analogue and digital signal processing in the same chip. This report provides the status at the end of the AIDA project and gives some prospects for the future electronics development.

# 1 Introduction

The realization of the readout electronics for the TPC in the ILD proceeds in three steps. The first step (EUDET) was to provide front-end electronics for the proof of principle phase, the aim of which was to demonstrate the feasibility of the Micro Pattern Gas Detectors (MPGD), GEMs and MicroMegas, with respect to the requirements set by the physcis challenges at the future Linear Collider. This step has been successfully completed. The electronics system set up for the EUDET project, based on the ALTRO readout electronics, provides very flexible test environment and if tests with really small pads turn out to be necessary the EUDET system should be used also in the future.

The second step (AIDA), which is presently ongoing, is the engineering phase with the aim of constructing an electronic system, which essentially meets the various requirements of the final front-end electronics. The electronics of the second step is based on the SALTRO16-chip, developed at CERN. (For a detailed description of the SALTRO16-chip and its characterization, see the theses of Massimiliano De Gaspari, http://archiv.ub.uni-heidelberg.de/volltextserver/13806/, of José García, http://riunet.upv.es/handle/10251/16980 and of Hugo Franca, http://cds.cern.ch/record/1563856/). The LCTPC-collaboration has obtained 610 such chips (210 as a contribution from CERN and 400 bought by Japanese groups). In order to achieve a significant reduction in size of the front-end electronics, a number of steps were introduced, performed for the first time with new equipment. In almost all aspects, it will require stretching the techniques beyond what is available in industrial manufacturing today. A tedious learning curve was expected, in particular since the malfunctions can be anywhere in the readout chain and thus are difficult to isolate. Thus, the development has been done in close cooperation with industry. The major complication arises from the fact that the SALTRO16 dies are delivered untested. Further restrictions are due to cost and availability of the chips, and that the yield is unknown.

The third step is to develop and produce the final electronics for the ILD.

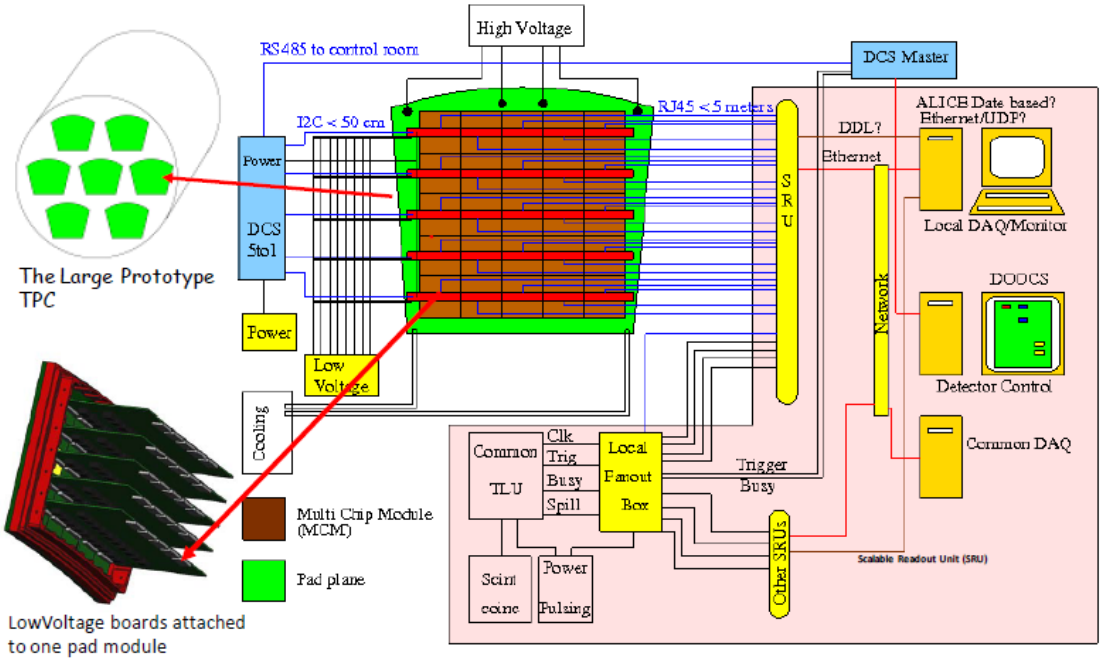


Figure 1: *Schematic view of the SALTRO readout system, shown for one pad module.*

# 2 The SALTRO16 Chip and the Carrier Board

The SALTRO16 readout system is schematically shown in Figure 1 for one pad module. It is a highly advanced development project, which includes several subsystems like the Carrier Board, the MCM-board, the Low Voltage Board, the Detector Control Boards, the Serial Readout and the Monitoring. A complication is that these subsystems (explained below) are not independent but have to be developed in parallel. In order to facilitate testing and debugging of the various subsystems, it has in some cases been necessary to construct prototype systems to avoid complications due to the requirements of compactness or due to other constraints. The Carrier Board and the MCM-board are especially challenging due to the tight space limitation and the high precision required. The project is performed in collaboration with industry partners, which have the necessary competence and experience. Due to the limited number of chips existing, the unknown chip yield and their high costs we had to take extreme care not to make any design errors and in the choice of industry partners, in order to minimize the loss due to fabrication failures. In the course of the development work, new ideas and solutions have been considered, that have led to improvements but also in some cases meant delays.

The SALTRO16 chip combines the analogue and digital signal processing of the incoming information. The silicon die itself is 8.7x6.2 $mm^2$ and contains 16 readout channels which equals an occupancy of 3.37 $mm^2$ per channel. The new chip can be turned off when no signals are expected, which reduces the power consumption and demands for cooling drastically.

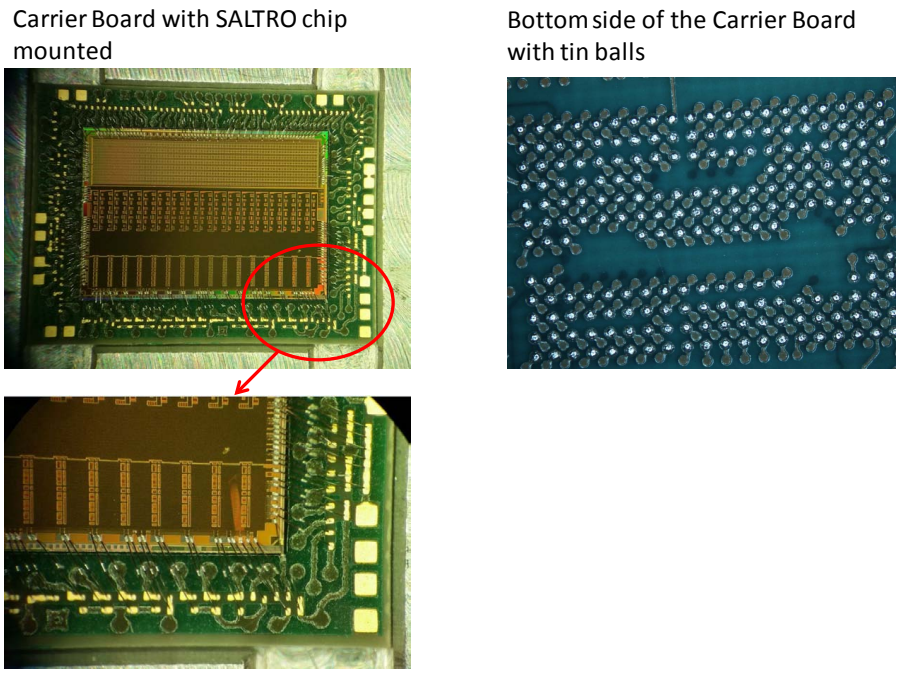


Figure 2: *A Carrier Board with bonded SALTRO-chip (top-left) and a blow up of one corner (left-bottom),where the bonding wires can be seen. To the right the bottom side is shown whith small tin balls applied.*

The alternative of using packaged chips is not a realistic choice since it requires too much space on the pad board in order to give small enough pad sizes, although testing, mounting and service would

be simpler. Due to the uncertainty in the yield it is unrealistic to assemble untested dies directly on a pad module and expect that all chips will work. Instead each die will be mounted onto an 8 layer Carrier Board, only slightly bigger than the chip itself, which simplifies the handling and allows individual chips to be tested. The size of the Carrier Boards is 12.0x8.9 $mm^2$, which also includes space for bonding wires, decoupling capacitors and other passive components. Eight of these carrier boards are mounted on one so called Multi Chip Modules (MCM) (see Section 5), using BGA soldering techniques.

A number of 250 Carrier Boards has been delivered. There are more than 200 bonding wires per board and the bonding procedure has to be very accurate, because of several bridge-overs, which require customized wire settings and fine tuning of the positioning due to the tightness. Figure 2 shows such a board before the application of the epoxy layer, which should protect the chip, the bond wires and the passive components.

# 3 The Test Set-Up

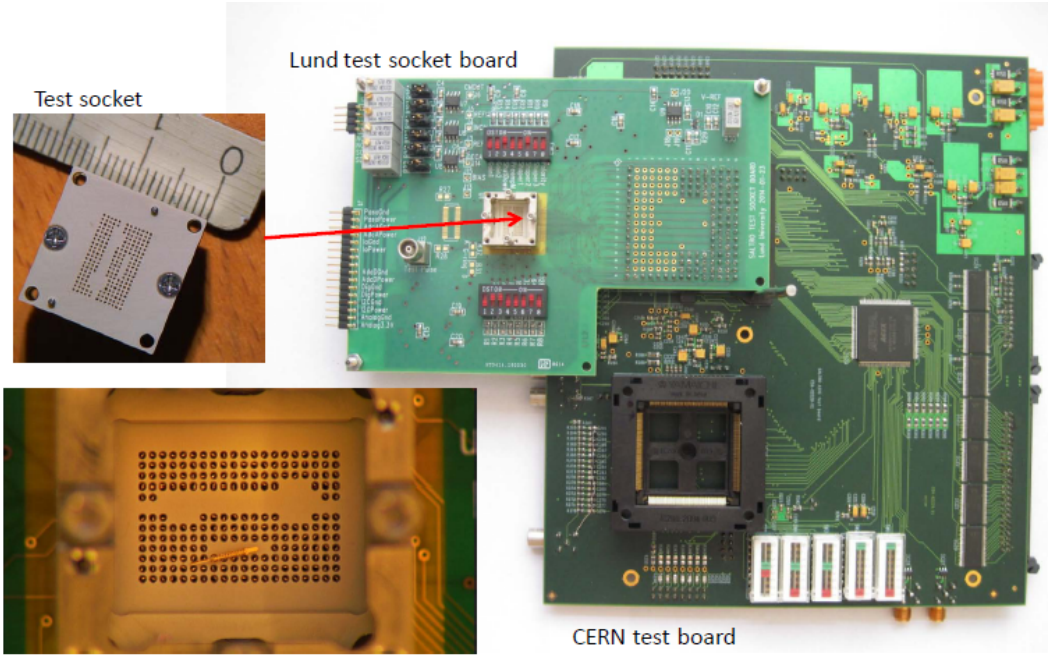


Figure 3: *Test Set-Up for tests of SALTRO-chips mounted on Carrier Boards.*

For functionality tests the Carrier Board, with a mounted SALTRO-chip, is placed in a test socket into which the Carrier Board fits exactly. The Test Socket is a commercially available, high technology product, which had to be customized to fit our BGA pattern. There are spring loaded probe pins guided by small holes in the bottom of the Test Socket, which make contact with the tin balls on the bottom surface of the Carrier Board. In order to secure sufficient contact of the 208 probe pins, a fairly strong force has to be applied from above. Thus, the epoxy glob must have a flat surface parallell to the board in order to distribute the force evenly over the whole surface. The height of the glob must not exceed $1mm$. Development of the globbing process was done on unmounted carrier boards to keep the waste of chips as low as possible. The application of the epoxy layer has caused

more problems than expected. In order to arrive at a satisfactory result various epoxy materials have been tried out as well as different application procedures and modifications of the moulding frame.

The application of small tin balls on the bottom side of the board has been successfully accomplished. The pins connect from the solder balls to the Test Socket Board, which has a matching BGA-grid and provides an interface between the Test Socket and pin grid array (PGA) socket on the CERN SALTRO test board. The CERN SALTRO test board was used to characterize the first packaged SALTRO16-chips. The Test Socket and the Test socket Board mounted on the CERN SALTRO test board are shown in Figure 3. The functionality of the CERN SALTRO test board has been verified using a packaged SALTRO-chip.

The assembled test system is shown in Figure 4.

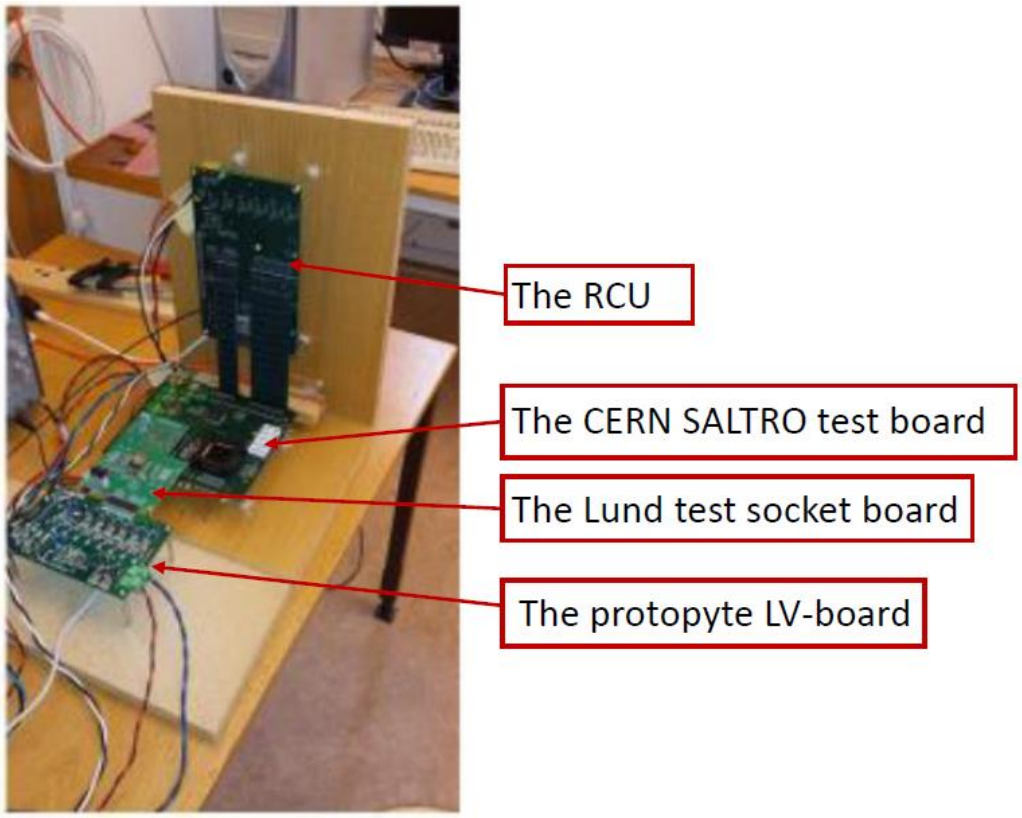


Figure 4: *The assembled Test Set-Up, also showing the prototype Low Voltage Board and the RCU.*

# 4 Test results

At the end of August 2014 the first completely mounted carrier board, with glob and tin balls applied, was delivered. A picture of this board is shown in Figure 5.

It turned out that the glob did not have straight edges, but some additional material on one side, that prevented the board to fit into the test socket. The additional material was carefully machined off until the board could successfully be mounted in the test socket. Due to the uneven surface of the glob, a piece of rubber material had to be placed between the upper surface of the glob and the lid of the test socket, in order to distribute the pressure reasonably even, so that all sensor pins got

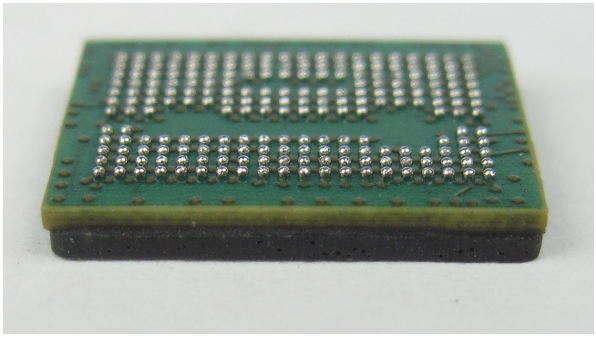

Figure 5: *The first fully mounted carrier board with glob and tin balls applied.*

contact with the tin balls at the bottom side of the carrier board. Evidently, the globbing of carrier boards, without chip and additional components, was not realistic enough and further development was needed for routine globbing.

Electrical tests of the board, with the machined glob, revealed that there were two pairs of shorted bond wires, which led the chip to enter an unstable mode so that no communication with the chip was possible. Furthermore, the sampling clock did not come through because of improper termination. After removing the board from the test socket it was noticed that the tin balls had some marks from the sensor pins of the test socket, but it is believed that this will not influence the soldering process.

Two additional fully assembled carrier boards were ordered and they were delivered in the beginning of December 2014. The quality of the globs was significantly improved. The edges were straight and the upper surface was without irregularities. No shorted bond wires were found but the sampling clock still didn't come through. The digital communication with the ASIC was established, while, lacking the sampling clock for the ADC, nothing was learned about the analogue part. The connectivity of the test socket and the functioning readout could, however, be verified, limiting the possible sources of error mainly to the carrier board with its SALTRO16 chip. It should be noted that it is expected that about 10% of the chips will have errors.

A naked carrier board was investigated for possible design errors, which might cause the systematic errors on the sampling clock. However, none were found and thus, a new fully mounted carrier board was ordered, with instructions that the company should document every step in the mounting procedure with high resolution photos and each step should be approved by us before the next step is performed.

The tight mounting conditions cause problems, which means that the company needs to improve their mounting procedure and that we have to be more actively involved in their process until it runs routinely.

# 5 The MCM-Board

The Carrier Boards will be mounted onto the MCM-boards by soldering of the small tin balls on the back side of the carrier board, organized in a so called BGA foot-print. Figure 6 shows the layout of the two sides of an MCM-board.

The advantages in placing the electronics components on separate boards, compared to soldering them directly onto the pad board, are listed below.

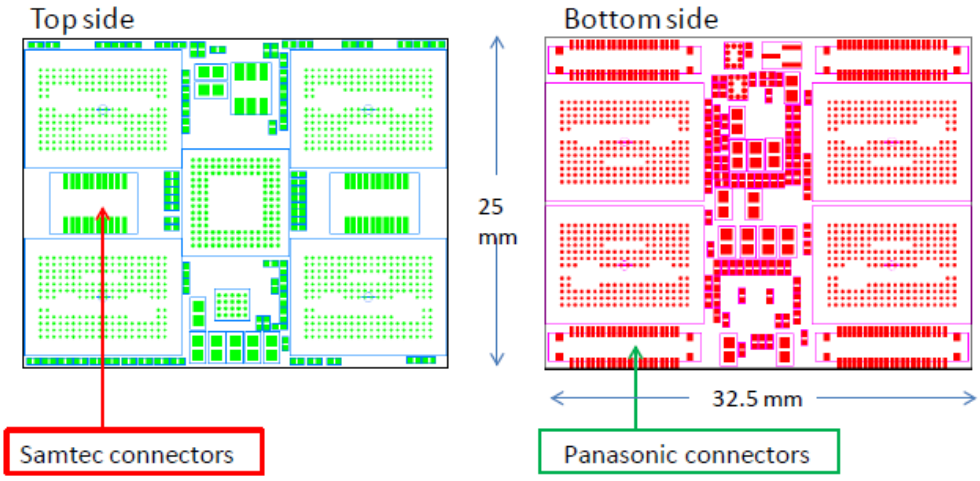


Figure 6: *The MCM-board top surface (left, green) and bottom surface (right, red)*

- Trace routing from the pads to the SALTRO chip becomes simpler since translational routing will essentially only be necessary at the edges of the pad module;
- With fewer or no active electronics components on the pad board it will be easier to design;
- Changes during the electronics prototyping will be cheaper and easier to implement and test;
- The interface between the SALTRO-part and the controller/readout-part is well defined;
- The trace routing on the plug-in board will be easier compared to the trace routing in the case all the electronics components are placed directly on the pad board. The pad board will need less layers;
- It moves heat away from the TPC endplate;
- It facilitates service. A malfunction in the readout chain can be fixed by replacing the electronics board instead of dismounting the whole pad board.

The MCM-boards will be attached to the pad board via 4 micro-connectors of type Panasonic, which have a lead pitch of 0.4 *mm* and a mated height of 2.5 *mm*, and transmit the signals from the pads to the preamplifier of the SALTRO16-chip. The connectors have to be mounted with very high precision on the pad board and on the carrier board since four such connectors have to fit simultaneously and the MCM boards are sitting very tightly. In order to meet the areal constraints, the Carrier Boards have to be mounted on both sides of the MCM-board. That is possible since the Panasonic connectors are elevating the MCM-board by 2.5 *mm* above the pad board, which thus leaves enough space for components on both sides of the MCM-board. In Figure 6 the rectangles with a dot-matrix of 20x13 dots are 8 sets of BGA patterns (4 on each side) for the SALTRO Carrier Boards. These boards are placed in each corner of the MCM-board such that the analogue inputs are facing outwards towards the long edges of the MCM-board, the bottom side of which the four 42-pin connectors for the 32 input signals (plus grounds) also are placed. The digital signals are concentrated towards the centre of the board. In the centrally placed square on the top side of the MCM-board, the BGA footprint of a CPLD (Complex Programmable Logic Device) is seen, which has an area of only 8x8 $mm^2$ (for details see Section 5.1). The total current drawn by the MCM-electronics is about 16 A per board at 8 different voltages, corresponding to a power consumption of about 22 W per board.

On the MCM-board there is also a DAC for setting the decay time in the preamplifier and reference voltages to the SALTRO16, as well as a temperature sensor. These are controlled via an I2C bus.

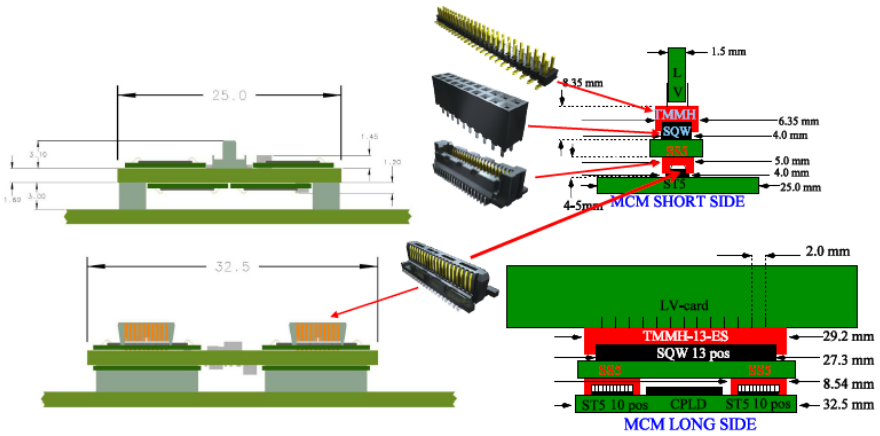


Figure 7: *Side views of the MCM-board assembly including an adaptor board.*

On the upper surface of the MCM-board Samtec connectors are placed for distribution of the low voltage and transmission of the signals from the SALTRO16-chip. The problem with this connector is that the female partner does not allow edge mounting on the LV-board, which has forced us to introduce an adaptor board, resulting in an additional pair of connectors. The MCM-board and the adaptor board is considered as one unit in the sense that it should not be needed to disconnect the two. The proposed layout of the adaptor board can be seen in Figure 7.

The dimensions of the MCM-board, which serves 128 channels, are 32.5x25 $mm^2$. This corresponds to a space occupancy per channel of about 6.4 $mm^2$. However, also some space is needed for HV-supply of the MPGD system and cooling of the electronics so that the available area for electronics is further reduced.

The MCM-board is designed in HDI-technology (High Density Interconnect). It is essentially ready and will be finalized as the tests of the carrier board have been succesfully completed, in order to take into account possible modifications in the design of the carrier board. The new HDI-technology allows for a higher routing density, including both signals and voltage supply, compared to conventional PCB design. This reduces the number of layers, which is favourable from a material budget point of view. From Figure 8 the high routing density can be appreciated. The Figure also shows a sectional image of the layer structure.

Thus the number of layers is reduced from more than 20 in conventional PCB design to 16 in HDI-technology. Vias are as small as 80 $\mu m$, made possible by laser drilling. The HDI-technology also offers the possibity to create cavities in the PCB, in which electrical or mechanical components can be mounted. These cavities are then covered with one or more dielectric layers so that the components are embedded into the PCB and the surface is essentially left free for surface mounting of readout chips. Such techniques are developed mainly for usage in purely digital applications. The main challenge for this project is thus to extend such assembly techniques to a system, which combines a highly sensitive analogue front-end with digital signal processing in the same compact circuit. Further challenges are the integration of the low voltage supply and cooling. Such solutions have to be discussed and developed in collaboration with industrial partners with expertice in assembly techniques.

We plan to produce a mock-up system to check that the mounting of the components and connectors on the MCM-board does not lead to unexpected difficulties and that the various parts fit together.

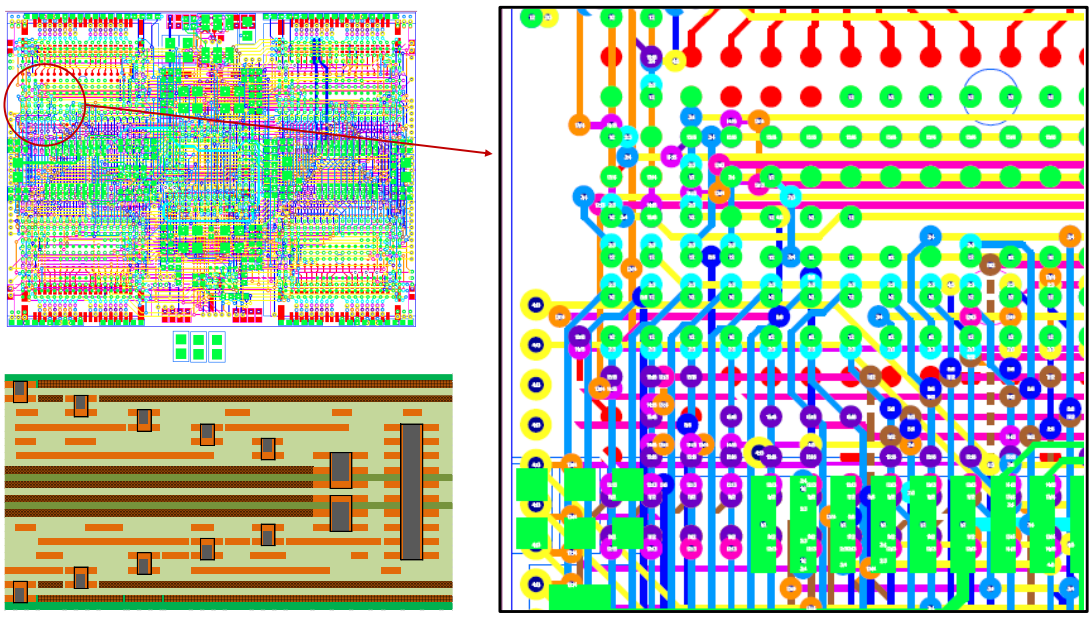

Figure 8: *The routing of the MCM-board using HDI-technology and a sectional image of the layer structure.*

## 5.1 The CPLD

The heart of the readout system on the MCM-board is the CPLD chip. There are four types of communication between the DAQ and the individual channels of an SALTRO16 chip.

- Send a command;
- Write data to a register;
- Read data from a register;
- Read the data of an event.

Most of these operations are concurrent during data taking and the control of the operations is handled via a serial link. Other controls on the MCM, which are done by the CPLD, are:

- The 8 bits for configuring the SALTRO16 preamp/shaper;
- Controlling the power pulsing of the SALTRO chip;
- Sending error and status messages to the DAQ

Tasks that do not need to involve the CPLD are foreseen to be done via the I2C communication from the 5to1-board through the LV-board. These operations include:

- Control the DAC for setting the pre-amplifier decay time and the SALTRO reference voltages;
- Reading the temperature sensors.

The CPLD will have two I2C interfaces, one for programming the CPLD, and one in the case we decide to communicate with the CPLD via the I2C as well.

The firmware for the CPLD is being developed by a group from Université Libre de Bruxelles (Belgium) and Hubei University of Technology (China).

## 5.2 The MCM Development Board

The MCM-board is a very dense board and not ideal for testing and debugging its performance. We have therefore produced an MCM Development Board, in a size of 210 x 145 $mm^2$, suitable for lab work. It is a stand alone board, containing only one SALTRO-chip in QFP package but also the necessary voltage regulators. Several testpoints and connectors allow for connection to a logic analyzer. The MCM Prototype Board is an 8-layer board of which 3 layers are signal layers and 5 power layers. This indicates the complexity of the power lines due to the many different power levels which are needed.

Three MCM Development Boards have been produced and the firmware for the CPLD has been installed. They have then been sent to Brussels, where the communication of the CPLD with the SRU has been verified. The packaged SALTRO-chips will be soldered and tests of the full communication will be performed. After this they will be distributed to the Lund-, Brussels- and Wuhan, where identical systems are set-up to improve the firmware of the CPLD (Brussels/Wuhan) and the Scalable Readout Unit (Wuhan), and to debug the system (Lund). The Scalable Readout Unit (SRU) will be described in section 7. The MCM-develolpment board is shown in Figure 9.

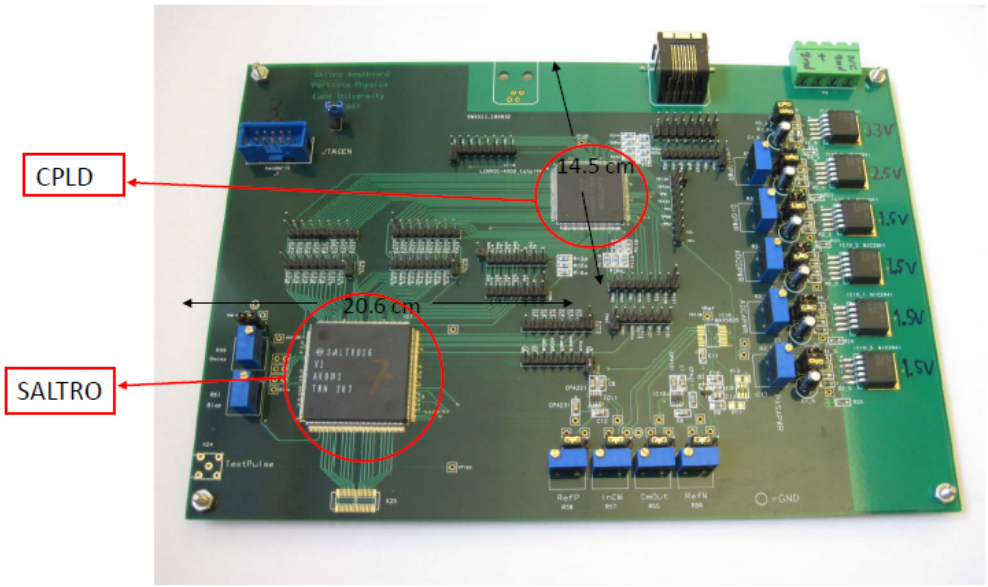


Figure 9: *The MCM Development Board.*

# 6 The DAQ-system

For the readout of the MCM-boards and communication to the DAQ we will use serial readout. The functionality needed locally in the vicinity of the MCM-board is the serial to parallel conversion of the downloaded data and the parallel to serial conversion of the uploaded (readout) data. This is accomplished by the CPLD chip.

Serial high speed readout has become possible with the development of a new generation of FPGA's that provide serial interfaces supporting data rates of several Gbit per second. A rather general purpose serial connection suitable for many experiments is the SRU (Scalable Readout Unit) developed in RD51. We plan to use the SRU to directly communicate with the MCM via the Data Trigger Control

(DTC) link, which contains clock, trigger/control and data. However, this requires that the FPGA firmware on the SRU is modified to include also the customized communication to and from the MCM. The MCM Development Board is used to test the firmware and to establish the communication between the SALTRO16-chips and the SRU.

# 7 The SRU

One SRU can handle 40 MCM-boards. The DTC protocol uses the four pairs of leads in the RJ45 cable for the fast signals. The solution reading the MCM-boards directly to the SRU is the cheapest as it uses the least new hardware.

There are two readout possibilities of the SRU, either the ALICE DATE with the DDL optial link or direct readout using optical ethernet.

One SRU with power box and cables have been purchased and the first tests have been successfully performed in Brussels. Thus, the communication between the SALTRO-chip and the CPLD was established as well as with the SRU. Although data could be read out, using the DDL optial link, it turned out that the data were corrupt, since the firmware for the SRU was not adapted to our system. To avoid being dependent of the ALICE DATE DDL libraries, the ethernet option is preferred.

# 8 The Low-Voltage Board

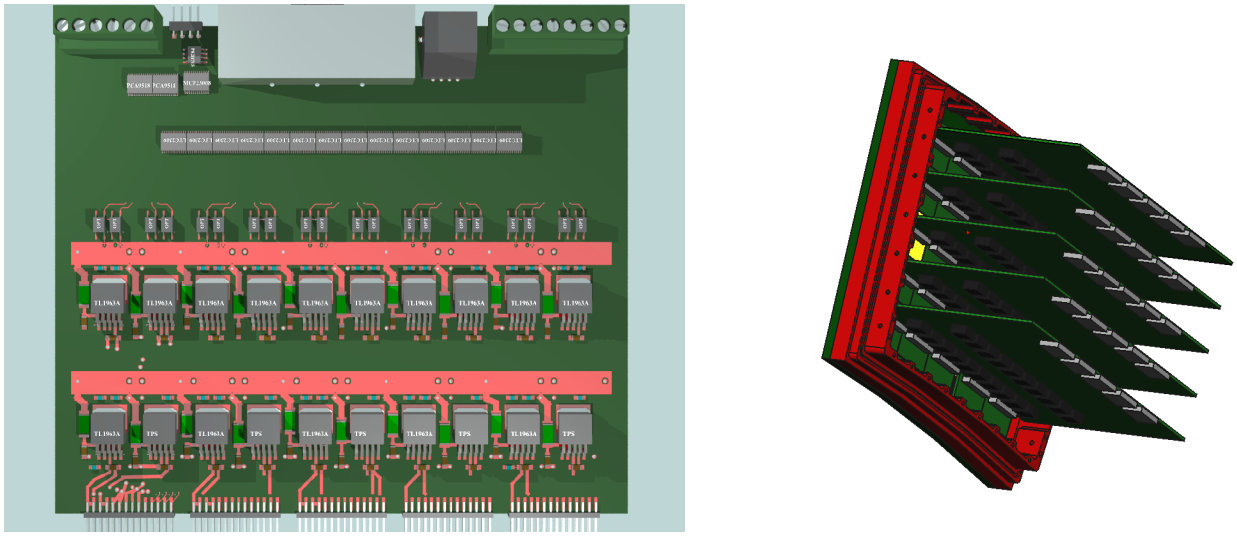

Figure 10: *The concept of the LV-board (left) and five LV-boards mounted directly on the MCM-boards of one module (right).*

The LV-board provides low voltage for five MCM-boards. Each MCM-board requires eight different voltage levels and thus the LV-board contains 8x5 = 40 voltage regulators. The communication with the CPLD and the I2C bus on the MCM is transmitted through the LV-board. There are five LV-boards per pad module. The board contains I/O registers to switch on/off the regulators, ADCs to monitor voltages and currents, and a temperature sensor.

The overall layout of the LV-board is ready and shown in Figure 10 (left). The maximum width of the board is limited by the dimensions of the module and the minimum width is given by the positioning of the connectors to the MCM-boards, which in turn depends on the layout of the cooling pipes. The final dimensions and layout, thus, still have to be fixed before the design can be completed. The LV-boards are connected to the MCM-board via the adaptor board. No cables will be used, which probably simplifies and speeds up the assembly procedure, as will be tested with the mock-up system. Such a system is also be favorable from a noise point of view. A schematic view of a module with five mounted LV-boards are shown in Figure 10 (right).

## 8.1 The Low-Voltage Prototype Board

The LV Prototype Board provides voltage for one MCM-board and is used to debug the design of the LV-board. Further it will provide voltage and some configuration to the Test Set-Up for testing the SALTRO16-chips on the Carrier Boards. The LV Prototype Board is ready and has been used to verify the I2C communication with the Detector Contol Boards (see Section 9) and the Test Socket Board to be used in the Test Set-Up. The board can be seen in Figure 11.

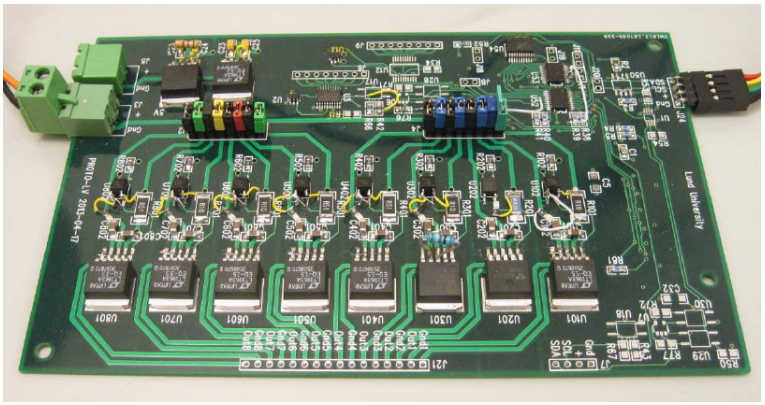

Figure 11: *The LV Prototype Board.*

# 9 The Detector Control System

In order to control and monitor the LV-boards and the MCM-boards, we have designed two boards, a master control and one slave module (called 5to1) both containing microprocessors. The slave module contains one microprocessor per LV-board for one pad module. The master board contains one microprocessor only, which can communicate with up to four 5to1 boards. A schematic view of the system is shown in Figure 12 (left) together with the corresponding boards (right). The boards are ready and have been succesfully tested.

We plan to monitor about 700 parameters from the LV- and MCM-boards per module. For this we are proposing to use DOOCS, which is already used by the DESY LCTPC-group with good experience. Oliver Schäfer from Rostock University has agreed to install our system into DOOCS. Software for the system is currently being developed.

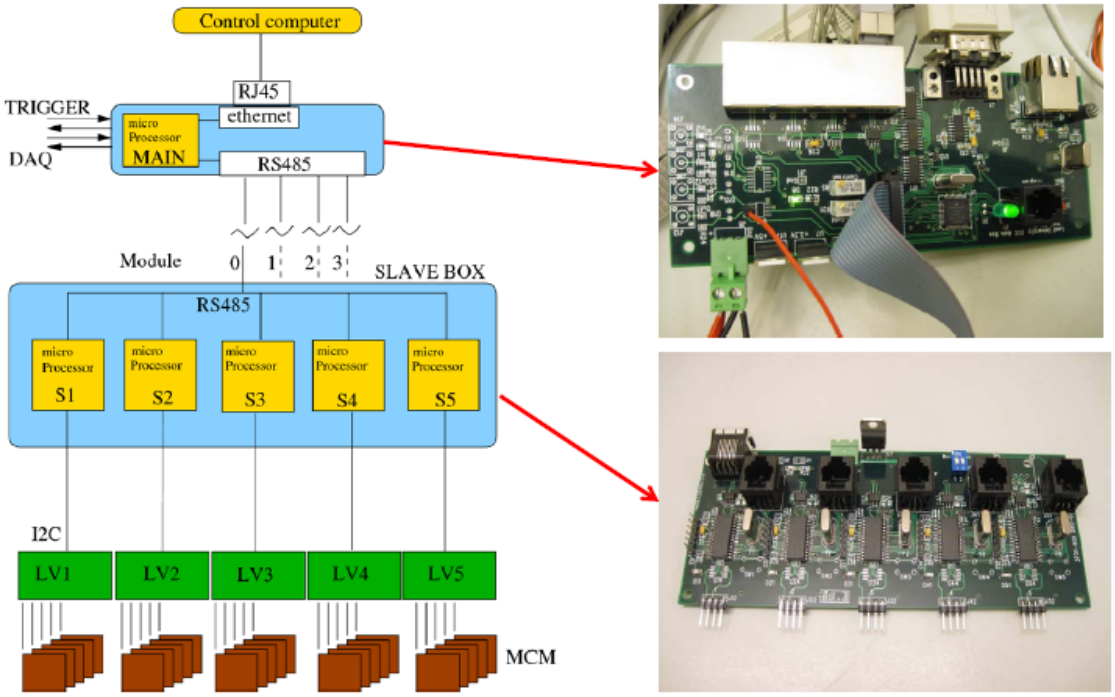


Figure 12: *A schematic view of the Detector Control System (left) and the corresponding boards (right).*

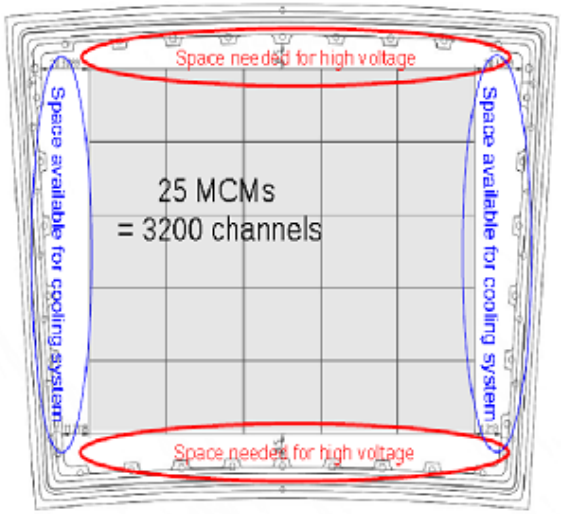


Figure 13: *The layout of the MCM-boards on a pad module with spaces for HV connectors and cooling indicated.*

# 10 Readout of a Pad Board

Figure 13 shows how 25 MCMs are arranged on a pad panel in a 5x5 matrix, which thus contain 128 x 25 = 3200 channels in total. This is consistent with a pad size of about 1x8.5 $mm^2$. The layout leaves some space on the sides as well as on top and bottom for the connection of HV-cables and cooling pipes, although the limited space probably will call for some innovative solutions.

# 11 Cooling

Cooling of the front-end electronics is an important and challenging issue. The dimensions of the cooling system should match the smallness of the electronics and still provide effecient cooling. For feasibility in the final detector, also surrounding equipment has to be taken into account. In the present EUDET-system air cooling is used but this is far too bulky.

From the characterization of the SALTRO16 chip at CERN it was found that the total power consumption per chip is 757 $mW$, i.e. 47.3 $mW$ per channel. An MCM-board contains 8 SALTRO chips and one CPLD. The power consumption of the CPLD is approximately 175 $mW$ at a sampling rate of 20 $MHz$. This gives a total power for the MCM board of 6231 $mW$. There are 25 MCM boards on a pad module, distributed over an area of about 215 $cm^2$, which leads to approximately 725 $mW/cm^2$.

Presently cooling with two-phase $CO_2$ is considered, with cooling pipes between the pad board and the MCM-boards. A test system has been set up by our Japanese partners to investigate the optimal routing of the pipes, the pipe diameter, the necessary flow rate and operational pressure, and various materials to insert for providing good thermal contact between the cooling pipes and the electronics. Tests with a mock-up system together with simulations have shown that the cooling capacaty of such a system is not suffient for continous operation of the readout electronics, but power pulsing has to be applied. ILC will according to the baseline design have a collision rate of 5 $Hz$. The bunch trains have a length of 725 $\mu s$ and contains 1312 bunches, i.e. there is about 199 $ms$ between the bunch trains. Operating the SALTRO chip in power pulse mode has shown that the power consumption is reduced to 9.2 $mW$ per channel. The CPLDS cannot be powered down since it is needed to start up the SALTRO chips again. Thus, it means that the total power of about 29 $mW/cm^2$ has to be cooled away in power pulsing mode.

An even more attractive solution is offered by microchannel cooling developed by the semiconductor community for cooling of IC chips. Microchannel cooling is well suited for high heat flux removal from electronics, like high performance computer chips. It provides an efficient way to remove heat from a surface and returning it to the cooling system before the coolant reaches the stringent temperature rise limit. The principle is that the heat generating chip is cooled with a primary fluid circulated in the primary heat exchanger that is in thermal communication with the chip. The primary coolant is cooled in a secondary heat exchanger by a secondary coolant from a secondary cooling system. The coolant in the primary loop may consist of either single phase coolants (water or refrigerants) or two-phase coolants (e.g. $CO_2$). By using refrigerants one can avoid the concern of bringing water close to the chip. There is an internal thermal resistance between the thermal contact surface and the chip, but this is in general low due to the high thermal conductivity of silicon and the short thermal paths.

In our case micro-channels might be built into the glob on top of the chips. Issues that have to be addressed before the system is implemented, are the circulation of the coolant during operation, leakage concerns, and channel blockages due to particulates.

Microchannel cooling is also considered for implementation in the vertex detector of the ILD experiment at the ILC (see talk by Ladislav Andricek, MPG, Munich on 'DEPFET based ultra-light all-silicon modules for vertexing at a future linear collider',
http://agenda.linearcollider.org/event/6389/session/4/contribution/166/material/slides/1.pdf), by integrating micro-channels in the silicon modules using etching. The first test results are very encouraging.

# 12 Mechanics

The aim is to find a solution that satisfies the needs of everything that have to be attached to the padplane (electronics, HV-cables, cooling etc.) The first ideas on a support structure for the electronics are illustrated in Figure 14. It is an Aluminum structure with grooves in the side walls to guide the LV-boards in position, such that the connectors of the LV-boards fit with the connectors of the MCM-boards. The open structure on top and bottom will provide some access during the mounting procedure. The LV-board has to be cooled but the design of the cooling system still has to be discussed.

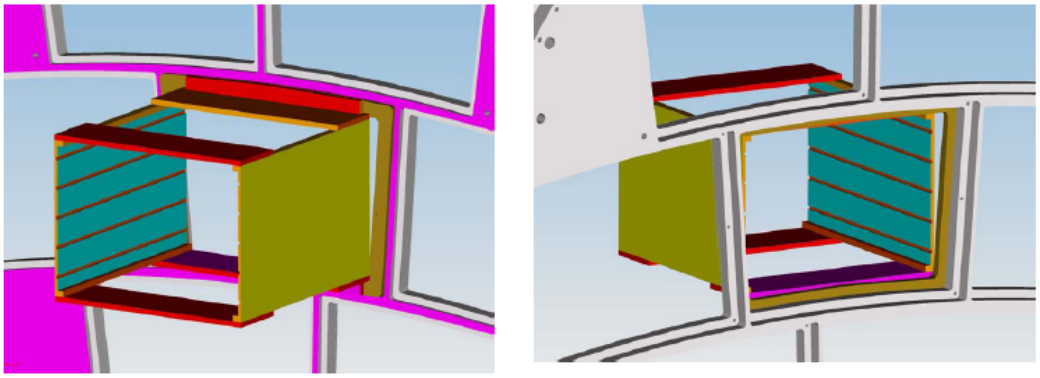

Figure 14: *First ideas on mechanics.*

# 13 Experience so far

The SALTRO16-chip does not provide an ideal solution for our application and has led to several cumbersome compromises in the PCB design. The disadvantages of the SALTRO-based system are for example the numerous connectors that are needed to link the various subsystems, the many voltage levels, which have led to a clumsy voltage supply system, and the many chip configurations that have to be set externally.

Since it is not likely that a final readout chip will be developed within the next years, further improvements of the PCB design have to be based on the SALTRO16-chip. Using novel techniques in PCB design, including 3D mounting of chips and possibly HDI (High Density Interconnect) technology, it will still be possible to construct front-end electronics that meets the requirements of small pad sizes. However, the SALTRO16 chip can not constitute the final solution due to the insufficient sampling depth.

# 14 Summary and next steps

The Test Set-Up for testing SALTRO16-chips, mounted on Carrier Boards, is assembled and has been used for tests of the first chips.
Three Carrier Boards with bonded chips have been tested so far. Some problems have been identified which have been communicated to the company. Another carrier board has been ordered.
A mock-up system with dummy Carrier-, MCM- and adaptor boards will be produced in order to test

the soldering procedure and verify that the various parts fit together.
The MCM-board has been redesigned using the HDI (High Density Interconnect) technology.
The design of the final LV-board can only be completed as the layout of the cooling pipes has been decided on and the dimensions of the mechanical support structure are settled.
Further development of the firmware for the CPLD and the SRU will be performed by Brussels and Wuhan. In Lund the software for the DAQ will be written and tests of the full readout chain performed.
An Ethernet based DAQ system will be developed and integrated in the common DAQ.
All these activites are going on in parallel.