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A CCD-based Vertex Detector for the Future Linear Collider

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Abstract

The future Linear Collider will provide a major challenge and opportunity for flavour identification. The small-radius beam-pipe and advances in detector technology will yield unprecedented performance for *b*- and charm-tagging, as well as more sophisticated tools such as the separate identification of quark and anti-quark jets for both *b* and charm. There are several technologies which may deliver the required performance, which comprises a combination of very small pixels (for clean 2-track resolution in the core of jets), excellent mechanical stability (to permit $< 5\,\mu$m overall measurement precision) and thin layers for acceptable multiple scattering of low momentum tracks (preferably $< 0.1\%\ X_0$). The CCD technology, building on the 307 Mpixel SLD vertex detector, offers one promising approach. This paper outlines the conceptual design of such a detector, updated in the light of the first year of an R&D programme which will continue for about another 6 years. The goal is to produce full-sized prototype detector components (barrel staves, or 'ladders') of which the performance will be compared with other silicon pixel technologies, in order to choose the one which best serves the physics requirements at the new machine. We include some observations generic to all technologies on such issues as correlated double sampling, beam-associated pickup and power dissipation.

1 Introduction

LEP, SLC and the Tevatron have established the importance of vertex detectors in understanding the physics accessible at high energy colliders. At the future Linear Collider (LC), both precision measurements and particle searches set stringent requirements on the efficiency and purity of the flavour identification of hadronic jets, since final states including short-lived *b* and *c*-quarks and τ-leptons are expected to be the main signatures. High accuracy in the reconstruction of the charged particle trajectories close to their production point must be provided by the tracking detectors, in particular by the vertex detector (VTX) located closest to the interaction point, in order to perform the reconstruction of the topology of vertices in the decay chain of short-lived heavy flavour particles in a complex environment. Low efficiency would be unacceptable due to the small event samples in individual processes, and low purity would generally be unacceptable due to backgrounds.

Experience at LEP and SLD shows the way forward. Jet flavour identification can be based primarily on the topological vertex structure in the jet, since this in principle allows most *B* and *D* decay modes to be detected. By aiming for good sensitivity down to decay times short compared with the mean lifetimes, high efficiencies may be realised. Distinguishing clearly between *b* and *c* jets requires additional information. This comes from the secondary and tertiary vertex topology, the charged decay multiplicity and the vertex mass, after applying corrections for missing neutrals, as implemented in the ZVTOP program [1]. One-prong decays of *B* and/or *D* mesons require special algorithms which are still under development.

As well as tagging *b* and *c* jets, the *vertex charge* (if non-zero) can distinguish *b* from $\overline{b}$, and *c* from $\overline{c}$. This requires sufficient precision to distinguish between all the decay tracks and those coming from the primary vertex. Even the case of neutral *B* decays can be handled by measuring the charge dipole between the secondary and tertiary vertices, as demonstrated in SLD, though this analysis is complicated by $B/\overline{B}$ mixing.

With the excellent calorimetry envisaged at the LC, reconstruction of high energy π^0s and their association with decay vertices (based on kinematics) may be efficient. If so, this may considerably enhance the ability to distinguish between *b* and charm jets.

Cases where leptons (and hence neutrinos) are absent from jets are particularly valuable for precise jet energy measurement. However, the absence of a single electron in a jet is not so easily established. Due to the prevalence of converted γs, it is important to track detected electrons inwards through the thin layers of the vertex detector to establish if they were really produced in semileptonic *B* or *D* decays. As well as providing a clean sample of jets free of missing neutrinos, this procedure in principle allows corrections to be applied to those jets which do include charged leptons (hence also neutrinos). In these cases, the jet energy measurement may be improved substantially by extending the procedure used in ZVTOP for the p_T-corrected mass, allowing a correction for the transverse momentum of the missing neutrino.

In short, careful control of backgrounds permits a small radius inner layer, making the LC interaction region particularly favourable for the construction of a vertex detector of unprecedented performance, well-matched to the physics goals of the TeV e^+e^- regime.

In Section 2 we discuss the physics motivation by means of a few typical examples, and in Section 3 we indicate how these lead to performance goals for the detector. In Section 4 we discuss the machine-related issues which influence the vertex detector design. Combining the performance goals with the restrictions from the machine leads to an acceptable compromise for the detector features, as discussed in Section 5. Section 6 discusses the CCD option in some detail, to the extent that the design has evolved to date. Section 7 discusses the question of pickup suppression and correlated

double sampling (CDS), an issue of importance for any silicon pixel detector with hundreds of millions of channels operating in a linear collider environment, where RF radiation in the region of the IR is inevitable.

How well does a detector that can be built, accessed and serviced satisfy the physics goals? The first step in addressing this question is taken in Section 8, where the generic performance in terms of 2-track resolution and impact parameter resolution is discussed. Further work on the evaluation of this detector for physics is addressed in [2] and [3].

The current status of the R&D work of the LCFI (Linear Collider Flavour ID) collaboration [4] is discussed in Section 9, as well as an outline of the plans for the next few years. In Section 10, we discuss the future outlook, including the tentative world-wide plans for convergence on one or two technologies to be selected for the first LC vertex detector(s).

2 Physics examples

If electroweak symmetry breaking is realised through the Higgs mechanism, the detailed study of the production and decay properties of the Higgs boson, in particular whether it satisfies the predictions for the Standard Model Higgs or some variant of SUSY Higgs, will require the future linear collider to measure its decay branching ratios with high precision. Precise measurements of the $b\bar{b}$, $c\bar{c}$, gg, $\tau\tau$ Higgs decay channels represents a major challenge for this detector system.

High energy WW production is a sensitive process with which to probe possible anomalies in the gauge boson self-couplings. To extract the full information, it is necessary to perform a complete angular analysis of the production and decay at the parton level. The favoured procedure is to analyse events in which one W decays leptonically and the other hadronically to $c\bar{s}$. The identification of the charm jet is essential for the analysis. The sensitivity of this analysis for new physics is strongly dependent on high charm tag efficiency and purity.

Efficient tagging and angular analysis of Ws is important in various supersymmetry scenarios, such as chargino pair production with

$$\tilde{\chi}_1^{\pm} \rightarrow W^{\pm}\tilde{\chi}_1^0$$

the signal being an acoplanar W pair in 4-jet final states. Charm jet identification is again important.

The scalar top (*stop*) sector may produce more complex final states where both b and charm tagging are important, such as

$$\tilde{t}_1 \rightarrow b\tilde{\chi}_1^+ \rightarrow bW^+\tilde{\chi}_1^0$$

Standard model processes such as high energy $t\bar{t}$ production provide equally challenging requirements:

$$t\bar{t} \rightarrow bW^+\bar{b}W^-$$

yields most frequently a 6-jet final state, two jets being b flavoured and frequently one or two more are charm jets.

The quantitative evaluation of the significance of flavour identification for these and many other processes requires a detailed study of the expected signals, backgrounds, angular information etc.

One delicate issue is the assignment of decay tracks to their correct parent jet in multi-jet events. This suggests a three-step process in which the jets are found initially, followed by vertex-finding within each jet, followed finally by the reassignment of tracks to jets on the basis of their parent vertices. Such algorithms are currently under development. While it is true that these studies are at an early stage, the SLD experience of the synergy between electron beam polarisation, high performance vertex detection and high performance calorimetry will clearly be extended with good effect into the TeV energy regime.

3 Performance goals

At first sight, the average impact parameter of a *B* decay product, approximately 300 μm (independent of boost for $\beta\gamma \gtrsim 3$) suggests that modest detector performance may suffice. However, this is misleading for several reasons. Firstly, the average impact parameters for τ and charm particle decay products are 3-4 times smaller. Equally importantly, in recent years the physics advantages have been established of detector systems which permit the correct assignment of nearly all tracks to primary, secondary or tertiary vertices. Determination of the vertex mass and charge are examples which permit greatly improved *b/c* separation and the classification of jets as *b* or $\bar{b}$, *c* or $\bar{c}$. The importance of the vertex detector in many physics analyses which go beyond simple *b*-tagging increases at higher collider energies with more complex events, each containing a large number of jets of various flavours.

The impact parameter resolution of a detector is a convolution of the point measurement precision, multiple scattering effects, lever arms and mechanical stability. One might hope that higher energy colliders would permit a relaxation of the concerns regarding multiple scattering, but this is not the case. Even in a 1 TeV e^+e^- collider, the average energy of particles in jets (depending on the physics process) is in the region 1-2 GeV. The most interesting events will probably have high jet multiplicity, where the problems are worst. Consequently, the detector design still needs to be pushed to the limit as regards layer thickness.

Independent of multiple scattering, the issue of photon conversions will become particularly important in the high multiplicity environment of the LC. A vertex detector having the thinnest possible layers, and which also allows standalone tracking, will certainly permit unprecedented cleanliness in the analysis. Electrons which track back all the way through the vertex detector are probably associated with semileptonic decay of heavy flavour particles, while those which do not are certainly the products of photon conversions.

Whatever performance is achieved for jets which are optimally oriented with $\theta \approx 90^o$, the impact parameter precision degrades at small polar angles due to the increased distance of the first hit from the IP, and the increased thickness of material traversed by the oblique tracks. For lower energy colliders, it was reasonable to restrict the analysis to say 90% of the solid angle. At the LC, this will no longer suffice, firstly because an event with high jet multiplicity will have a significant probability that one of the jets is found in the extreme forward or backward region, and secondly because much of the physics relies on having spin-polarised electrons and/or positrons, where the significance of events is weighted in favour of the forward-backward direction. Full coverage with at least 3 vertex detector hits is desirable over about 96% of the solid angle. Beyond that, lever arms become extremely unfavourable for high precision track extrapolation.

4 Machine-related issues

The luminosity and bunch timing at the LC, combined with the requirement of untriggered operation, impose particular constraints on the vertex detector. This is particularly challenging in the case of TESLA. Data need to be stored somewhere (preferably local to the detector) through the 1 ms bunch train, then transferred to the processor selected to handle the data for that bunch train. For successive trains, data are transferred to different members of the processor farm. It is not necessary for the data from the vertex detector to correlate with a unique bunch crossing. On the contrary, it is acceptable to accumulate the signals over a number of bunch crossings (as at SLD) provided that the hit density is everywhere sufficiently low that the track fitting is not significantly compromised. The CCD detector option takes advantage of this important trade-off, which favours high granularity and moderate readout speed. The optimal solution depends on the magnitude of the machine background. In TESLA, the dominant e^+e^- pair background from the beam-beam interaction is confined radially by the 4T magnetic field of the detector solenoid. Consequently, the background is strongly peaked in layer 1, and falls rapidly beyond; thus the readout of layer 1 needs to be the fastest. Due to constraints on the design of the machine collimation system, it is necessary to set the beam-pipe radius at 14 mm. The pair background in a vertex layer just outside this beam-pipe produces about $0.03\ \text{hits}/\text{mm}^2.\text{BX}$, which is acceptable for the foreseen readout system. There are 2820/4500 bunch crossings (BX) per train at 500/800 GeV, with a BX interval of 337/189 ns.

In the case of NLC/JLC, the background is accumulated in much smaller bursts of duration about 266 ns repeated at the bunch train frequency of 120 Hz. In this case, each bunch train can be considered to be an instantaneous small burst of luminosity and background, and the modest hit density accumulated during the train can be read out comfortably in the 8 ms inter-train interval.

Apart from the question of hit density in the data due to the background particle flux, one has also to consider the question of radiation damage to the detector. For both TESLA and the NLC, the dominant background (pair-produced electrons which penetrate the VTX inner layer) imposes a requirement on radiation hardness of about 100 krad for a 5 year life, which is easily achieved with modern CCD technology. Potentially more serious is the background from neutrons generated by various sources, primarily the beam dumps and the beamstrahlung dumps. This background is currently estimated to be of the order of 10^9 $1\ \text{MeV-equivalent neutrons}/\text{cm}^2.\text{year}$, which is acceptable with current CCD designs. There is furthermore scope for major performance improvements, which could lead to a large safety factor in radiation tolerance.

5 Detector features

It is now generally accepted (after numerous design studies) that the optimal layout for an LC vertex detector is a series of nested cylinders. This is not obvious, since long barrels imply large obliquity factors at the ends of the polar angle range, and one might be tempted to consider short cylinders plus ‘lampshade’ or endcap detectors. The basic reason to avoid this approach is the inevitable excess material budget imposed by the support structure and cabling of the vertex detector, which renders the endcap planes relatively useless for precise impact parameter extrapolation. Endcap detectors are of course vitally important, beyond the region of the vertex detector, in order to maximise the hermeticity for tracking, but when such detectors fall below the angular coverage of all layers of the vertex detector, they can play almost no part in heavy flavour tagging. As well as being shown from simulations, this limitation has been experimentally established at previous collider detectors.

The inner layer needs to be as close as possible to the IP. Given the overriding importance of this feature, the inner layer should extend in length to cover the full polar angle coverage of this detector system. With an inner layer radius of 12-15 mm defined by the final focus system, it is has been

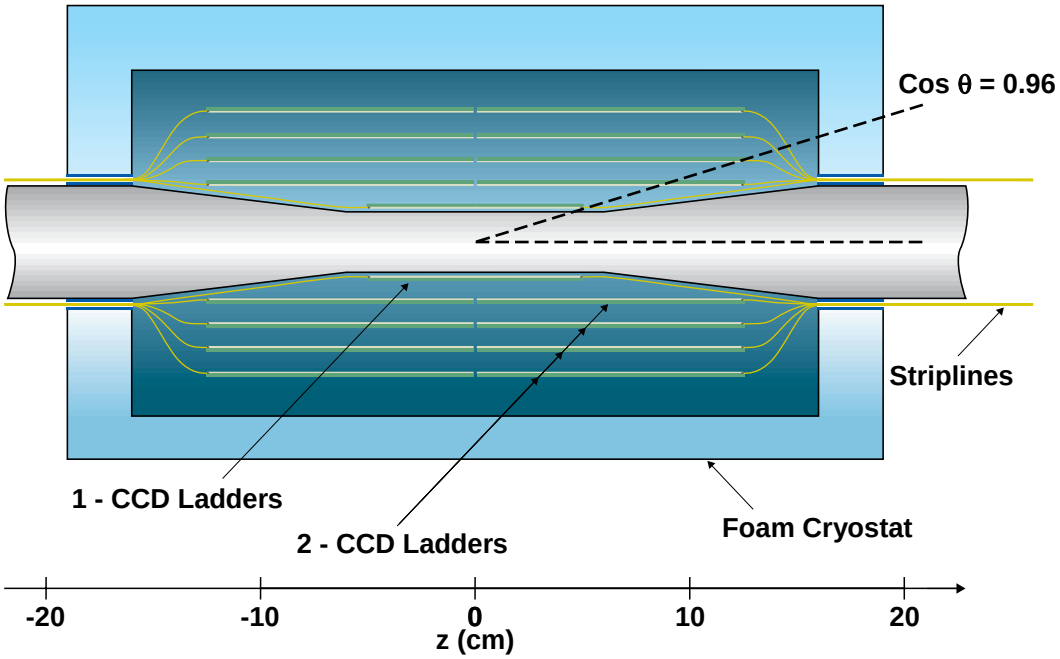


Fig 1: Cross-section of vertex detector. Cylindrical support shell linking the beam-pipe at $|z| \approx 15$ cm is not shown.

demonstrated [5] that a pixel-based detector with pixels of size well below $50 \times 50\ \mu\text{m}^2$ is required in order to avoid confusion (cluster merging) within the cores of high energy jets.

The CCD design is shown in Figs 1 and 2. The inner 3 layers extend to $|\cos\theta| = 0.96$, with 5-layer coverage to $|\cos\theta| = 0.9$. The outer 4 layers provide stand-alone track reconstruction. The advantages of stand-alone reconstruction in tracking sub-detectors are well-established; they include internal alignment optimisation, efficiency monitoring of the external tracking systems and vice versa, optimal detection of γ conversions within the vertex detector and optimal rejection of 'bad' hits due for example to merging between signal and background clusters.

Having found the tracks in layers 2-5 (and rejected a low level of fake tracks by linking to the outer tracking system) the layer 1 hits are used solely to refine the track extrapolation to the IP, which is particularly important for low momentum particles.

Figures 1 and 2 shows the detector inside its low-mass foam cryostat, which is used to permit an operating temperature of around 180 K. Not shown in the figures is the high precision mechanical support structure (a closed beryllium cylinder) which is mounted off the beam-pipe inside the cryostat. Being outside the volume used for the precision measurements and extrapolation to the IP, this cylinder can be relatively robust (approximately 2 mm wall thickness). It serves the additional role of clamping the two sections of beam-pipe rigidly together (clamps at z about ± 15 cm) so that the critical inner cylindrical section of beam-pipe of length 12 cm and radius 14 mm can be made extremely thin: 0.25 mm wall thickness beryllium is considered possible. Striplines carrying power and electrical signals are routed along the beam-pipe below the polar angle range used for tracking, connecting to small DAQ boards which are flat-mounted on the outer surface of the SR mask assembly.

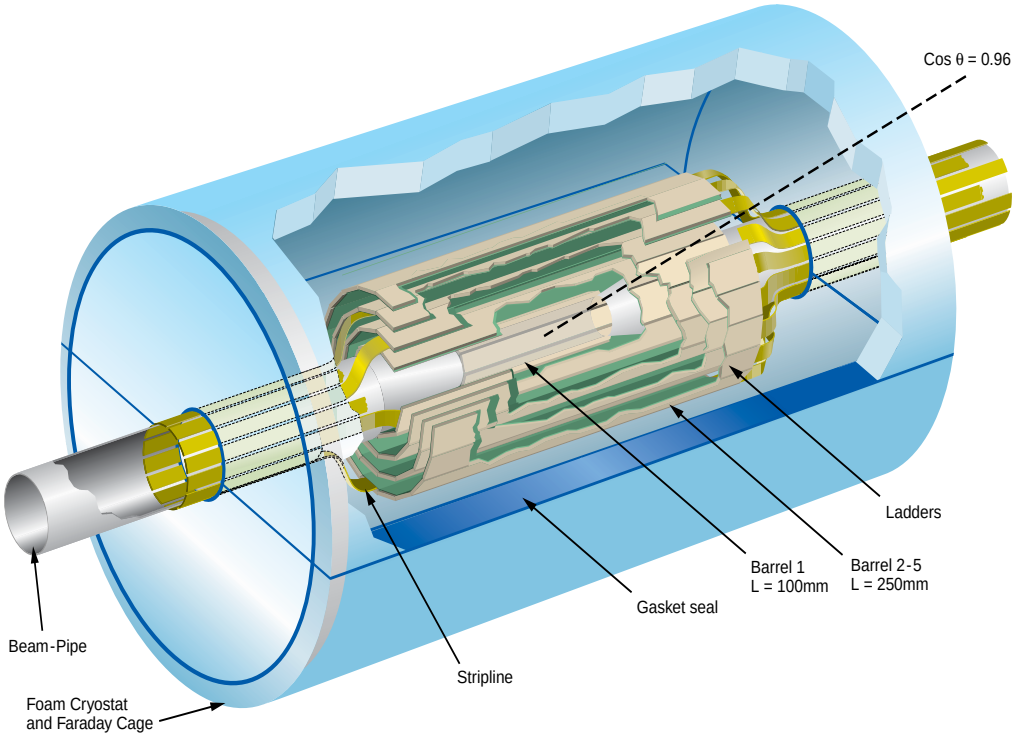


Fig 2: Isometric view of the vertex detector, again without showing the support shell

The vertex detector will be an extremely sophisticated part of the LC detector. Along with other elements of the inner detector system, it will potentially need periodic maintenance and upgrades. For this reason, there needs to be a clear plan for carrying out such operations without a major impact on other delicate equipment such as the final focus magnet system. A procedure for avoiding such interference has been devised, and is based on a strategy of rolling the outer tracking system along the beam-line by about 5 m, to provide access to the inner detector. This follows the procedure used successfully in the SLD experiment, where access was conveniently available for installation of upgraded beam position monitors and beam size monitors, as well as an upgrade vertex detector, during the life of the experiment.

6 Conceptual CCD-based detector design

In the case of NLC/JLC, the detector design can follow the principles established for SLD. The detection layer will consist of about 10-20 μm of silicon in the form of an epitaxial layer of relatively lightly doped material grown on a heavily doped p^+ substrate. The epitaxial material is depleted to a depth of only about 1 μm, with the signal from the minimum-ionising particle being collected into the buried channel of the CCD largely by diffusion. The charge collection time is ~100 ns, and is completed after the passage of the bunch train, before the start of detector readout.

For TESLA, the situation is more complicated. Due to the need for fast clocking of the signal charge throughout the bunch train, fast charge collection (~10 ns) is necessary. This can be achieved by using relatively high resistivity epitaxial material, depleted all the way to the edge of the epitaxial layer. Due to the Lorentz angle in the 4T solenoid field, the stored signal is dispersed 'horizontally' (across the CCD columns in $r\phi$ direction). Despite the 'vertical' clocking (in z direction) at 50 MHz, phasing of the clocks with the bunch crossings is expected to result in negligible vertical dispersion of the signal charge. Detailed optimisation of the pixel dimensions will depend on full 3-D simulation of

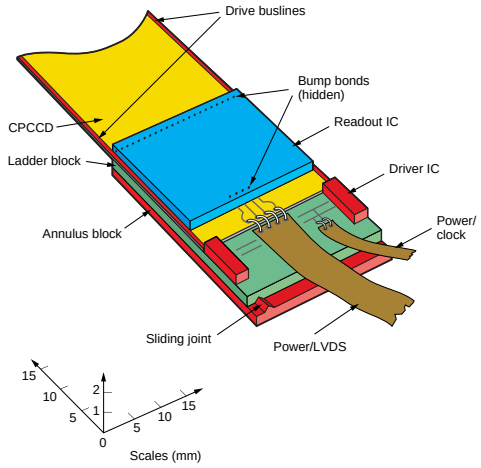


Fig 3: Layout of components at end of ladder

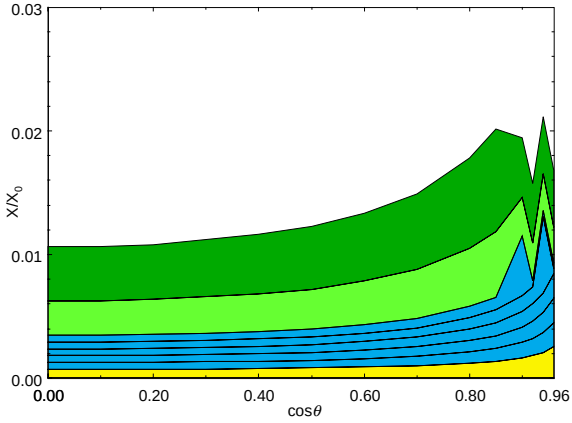


Fig 4: Material budget as function of polar angle
(beam-pipe, each of 5 layers, support shell and cryostat)

the charge generation, storage and transfer to the edge of the CCD, but it is expected that optimised values (horizontal, vertical and in depth) will lie in the range 20-30 μm .

For both detector designs, the p^+ substrate is useful only for mechanical purposes (handling, mounting, achieving sufficient mechanical stability). Depending on the overall ladder design, this substrate can be mostly removed by mechanical lapping and chemical etching, leaving a thin residual p^+ layer. On current thinking, the epi-layer thickness will be 20-30 μm , and the overall CCD thickness about 50 μm .

As shown in Figs 1 and 2, the ladders in layers 1-3 (CCDs attached to thin beryllium support sheets) comprise all the material in the critical fiducial volume out to $|\cos\theta|$ = 0.96, the limit of high precision tracking for vertex reconstruction. Material extending radially or longitudinally beyond this volume is less critical, so one can afford somewhat more substantial mechanical supports and readout electronics. This approach illustrates both the strengths and weaknesses of the CCD design. The advantage is unprecedented quality of impact parameter measurement, due to the minimal material and heat load, allowing the critical volume to be cooled by a gentle flow of nitrogen gas. The disadvantage is the requirement to transfer the signal charge packets out of the fiducial volume before they can be sensed. The innermost layer consists of single-CCD ladders, read out from both ends, while layers 2-5 are made of 2-CCD ladders, butted together and read out from the outer ends only. Thus in some cases signals of about 1000 electrons have to be transferred faithfully over a distance of up to 12.5 cm (~ 6000 pixels) en route to the CCD output. While this is a standard procedure for scientific grade devices, achieving this at high speed and in a non-negligible radiation environment is challenging. All the thin ladders are stabilised mechanically by being bonded to 'ladder blocks' which are able to slide along rigidly supported 'annulus blocks', the ladders being pinned at one end and held under tension by springs at the other (sliding) end as indicated in Fig 3. This support system extends the principles pioneered in the SLD vertex detectors [6,7]. As well as providing the mechanical support for the CCD, each ladder block carries the local electronics components in the form of two or three integrated circuits. The driver chip (see Fig 3) generates the waveforms which shift the stored signals row by row down the device. The readout chip receives the analogue signals from all columns in parallel as they are shifted out of the active area to buffer amplifiers. This chip incorporates analogue-to-digital conversion, correlated double sampling to suppress reset noise in the charge-sensing circuit, data sparsification by a sequence of pixel- followed by cluster-comparators, data storage and buffering to the external DAQ system.

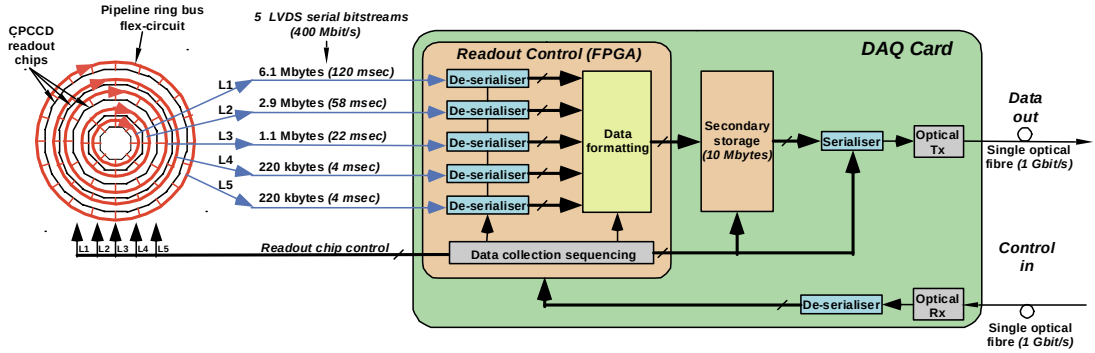


Fig 5: DAQ system at one end of vertex detector. LVDS signals are connected by flex circuits to each layer, and externally to a small DAQ card on the SR mask close to the VTX cryostat.

Some of the key parameters associated with the detector design are listed in Table 1. The number of pixels (799×10^6 in total) assumes a pixel size of $20\times20\ \mu\text{m}^2$. Processed data stored in the readout ICs during the bunch train, amounting to ~ 20 MB, are read out via a pair of optical fibres (one at each end of the detector) between trains. The essential features of the DAQ system are indicated in Fig 5. The power dissipation in the drive and readout ICs may exceed the capability of gas cooling. In this region, the material budget is less critical and one can consider a more robust cooling system, specifically evaporative nitrogen cooling as used successfully in the CCD vertex detector of the CERN NA32 experiment [8], the first particle physics experiment in which a pixel-based vertex detector was used.

The most ambitious scenario for ladder construction ('unsupported silicon') results in the material budget shown in Fig 4. The beam-pipe and critical first 3 layers amount to 0.25% X_0 at $\cos\theta = 0$ and rise to only 0.8% X_0 at $|\cos\theta| = 0.96$. The detector has 5-hit coverage to $|\cos\theta| = 0.9$, beyond which the end supports and electronics of layers 5 and 4 are encountered. The support shell and cryostat, while contributing material at all angles, are relatively benign, being beyond the region of high precision tracking. By the time the particles encounter this material, their impact parameters are well measured. While such a thin detector may prove to be too optimistic, the mechanical R&D programme described in Section 9.1 suggests that a material budget close to this goal of 0.06% X_0 per layer may be achievable, along with the required micron-level mechanical stability.

Layer	Radius	CCD L×W	CCD size	Ladders and CCDs/lddr	Row clock fcy and Readout time	Bgd occupancy	Integrated bgd
	mm	mm^2	Mpix			Hits/mm^2	kHits/Train
1	15	100×13	3.3	8/1	50 MHz/50 μs	4.3	761
2	26	125×22	6.9	8/2	25 MHz/250 μs	2.4	367
3	37	125×22	6.9	12/2	25 MHz/250 μs	0.6	141
4	48	125×22	6.9	16/2	25 MHz/250 μs	0.1	28
5	60	125×22	6.9	20/2	25 MHz/250 μs	0.1	28

Table 1: Key parameters of the vertex detector design. Background occupancy is based on calculated density per BX multiplied by number of BX during readout of that layer.

7 Pickup suppression, correlated double sampling and power dissipation

All LC vertex detector technologies imply fast sampling of the very small signals from hundreds of millions of silicon pixels. In principle a disturbance due (for example) to external pickup can create a fake signal in a pixel. Even at a level of say 10^{-4}, such pickup would severely overload the DAQ system and create track-finding problems, so it would need to be extremely efficiently suppressed. The technique of correlated double sampling (CDS) is used to achieve this, and is equally applicable to CCDs, DEPFET and MAPS systems. CDS is a form of baseline restoration originally developed to suppress reset noise in CCD readout systems [9]. In its simplest form, the front-end of a CCD readout circuit consists of a small on-chip transistor (usually connected as a source follower) whose input gate is connected to the output node onto which the signal charge is transferred. Prior to each charge transfer, the potential of the output node is reset to some standard value, so the signal is determined by the difference between the measured reset voltage and the voltage following the charge transfer. However, the reset potential expressed in equivalent noise charge (ENC) inevitably fluctuates by $\sqrt{kTC_N}$ coulombs, where C_N is the node capacitance. For a typical CCD node capacitance of some tens of fF, this noise source amounts to some tens of electron charges, which would totally dominate the readout noise in typical scientific slow-scan readout systems. By operating the CDS differencing procedure, and by appropriate shaping (e.g. dual slope integration) of the signals before sampling, overall noise of a few electrons ENC can be achieved.

In the case of a CCD-based vertex detector, the CDS functionality can be provided without the inconvenience and speed penalty of resetting before each charge transfer. One can for example reset only once, at the beginning of the bunch train, then take successive samples after each charge transfer, with the signal for each pixel being given by the difference between successive samples. For this to work properly, the integrated signal during the bunch train should not drive the analogue or ADC circuit into saturation. This condition may well be satisfied in the sparse data conditions associated with a tracking detector (in obvious contrast to a focal plane imager in astronomy, where spatially extended bright objects are frequently encountered). If the system would run into saturation, as may be the case on the innermost layer at TESLA, further refinements such as a long time-constant recovery to the baseline via a high resistance load may be considered.

When implemented in this manner, the front-end CDS circuit can also provide powerful suppression of noise or pickup. The primary function of reset-noise elimination is achieved by measuring the steps between successive samples. The additional noise-suppression feature called extended-row filtering (ERF) [7] can be understood by reference to Fig 6. The principle is that whereas a valid signal causes a step in the node voltage, pickup spikes or rare (many standard deviation) noise fluctuations will normally be restricted to one sample. The complete row of data is digitised, and the signal associated with each pixel is taken to be the minimum of two overlapping samples as shown in Fig 6. These two samples will be closely similar for valid data, but one of them will be approximately zero (and hence cause the global estimate to be discarded as below threshold) in the case of noise. This procedure was effective in suppressing the noise/pickup rates in the SLD experiment by about a factor 100, leading to comfortable data rates from a detector of 307 Mpixels [7].

The column parallel CCD design should be particularly robust with respect to pickup suppression, more so than the SLD detector. The signal charges from remote regions of the detector are physically transported (noiselessly) to extremely compact signal-sensing circuits on the periphery of the CCD, consisting of output node (a reverse-biased diode), source follower, amplifier and ADC (linked by very compact bump bonds) all contained in a space of about $20\mu\text{m}\times 1\text{ mm}$. However, in SLD the amplifier boards were displaced tens of centimetres from the CCD, connected by long copper/kapton striplines, and hence relatively susceptible to pickup.

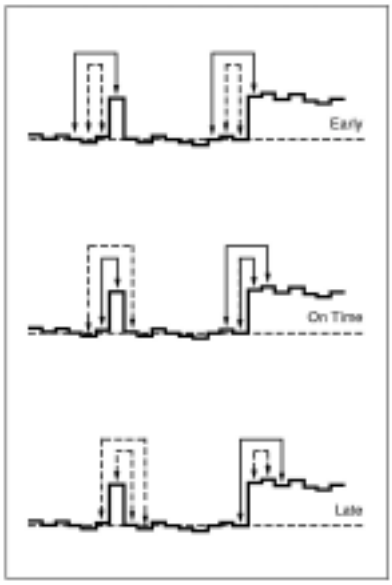


Fig 6: Extended row filter operating on a row of digitised CCD data. Whereas both overlapping samples register a hit when 'on time' for valid data, this never happens for the pickup/noise spike.

Some MAPS architectures (Flexible APS or FAPS) [10] could be equally robust. Others involve sending analogue signals along long column buslines to charge sensing circuitry near the chip edge, and these could be more vulnerable to pickup. However, both these options operate their CDS on a 'rolling shutter' basis, with the period between samples being the frame readout time, say 50 μs, in contrast to a fast-running CCD where this may be 20 ns. The MAPS architecture would be much more sensitive to pickup and baseline fluctuations, in this example. The DEPFET approach [11] consists of sensing the signal, then draining the entire signal charge out of the potential well which comprises the internal gate, and sensing the reset level which results. This could permit as clean and fast an implementation of CDS as with the CCD readout, though without the added benefit of the enhanced pickup suppression via the ERF logic, though this could be added at considerable expense in terms of readout time.

There are other factors, independent of the vertex detector technology, which may dramatically alter the issue of external pickup. In SLD, the incidence of fast spikes was considerably reduced when the vertex detector was installed in the main detector barrel, with the doors closed; 6000 tons of iron in a hermetic configuration provides extremely effective RF screening. The CCD cryostat was in addition fitted with a thin-walled Faraday cage on its inner wall, including a re-entrant section to screen out RF being piped in along the beam-pipe. However, whereas the detector could be read out quietly in the absence of beam, there were major spikes of RF radiation coincident with the bunch crossings. While these did not affect the CCD readout directly, since this was gated off for a few μs after the beam crossing, the pickup did dislocate the phase-lock loop of the optical converters. Fortunately, they could be reset within about 100 μs, so the readout was barely affected.

The source of these RF spikes was never tracked down. It is unlikely to have been the beam-associated image current directly penetrating the beryllium or stainless steel sections of beam-pipe. However, bellows regions, BPMs and beam-size monitors penetrating the beam-pipe, could well have provided leakage paths through which a small fraction of the ferocious beam-related RF radiation could escape.

In the case of NLC/JLC, one can follow the same general approach that worked at SLD. Large beam-associated RF spikes may well be encountered during the bunch train, but there will be plenty of time to reset the entire readout system to its standard condition before starting the sequence, given the 8 ms interval between bunch trains. The signals deposited in the detector are accumulated safely in the potential wells of the buried channel of the CCD throughout the bunch train. This storage mechanism is extremely robust, and completely immune from external pickup.

In TESLA, the situation is more complex. Due to the need for multiple readout of the detector during the bunch train, the entire readout system (charge transfer, analogue amplifier, analogue-to-digital conversion, digital processing and data sparsification, optical conversion and fibre readout) must continue functioning at full speed throughout the train. This requirement (which will be shared by all the VTX technology options) is unprecedented at a linear collider. It would have been impossible with the VTX electronics used at SLC, and will probably be a considerable challenge.

Whichever accelerator technology is chosen, it will be necessary to construct a 'Final Focus Lab' in which prototypes of the different small-radius detector systems can be assembled and tested for compatibility, in a mechanical, thermal and electrical replica of the LC beam delivery system. The beam-associated pickup can be simulated by current pulses down stretched wires. In the case of TESLA, such testing will be essential, in order to establish viability of any of the candidate VTX technology options in this novel and challenging environment. It is possible to make hand-waving arguments about compact systems being potentially robust, but all circuits at least have bias lines attached, running to the ends of the ladders, so there is always the risk of RF interference. Such effects are notoriously difficult to simulate, and at least one vertex detector in the past has been rendered unusable due to beam-related pickup. As the complexity of the systems increases while their size shrinks, it is not entirely obvious whether the problems will become more or less severe.

Another topic of serious concern for all vertex detector technology options is power dissipation. In SLD, the average power dissipation in the detector volume was about 15 W. In this case, the only power of importance was generated on the CCDs themselves, since the driver circuits and readout electronics were all located in the small-angle region close to the SR masks, below the coverage of the tracking systems. In this location, water cooling of the electronics was used since the material budget requirements were not critical.

For the future LC in the TESLA option, it is planned to move the drive electronics to the ends of the ladders and to attach the readout electronics also locally, bump-bonded to the CCDs themselves. So the increased power dissipation is moved into the cryostat, though not into the most critical fiducial volume for precision tracking.

As in SLD, it is expected that the CCDs will be cooled by a gentle flow of nitrogen gas. It is not entirely obvious that this will be possible, because of the much higher clocking rate of the parallel register. But it is hoped to reduce the clock amplitudes to 1-2 V, and to use 'metal buttressed' gates to minimise on-CCD resistances. These two steps will suffice to retain the possibility of gas cooling, with the obvious advantage of no excess material (coolant pipes, liquid coolant) in the fiducial volume. For the ladder ends, present indications are that the readout ICs will dissipate extremely little power, but the driver ICs will necessarily be significant sources of heat.

This problem can be greatly diminished, if not solved completely, by the use of 'pulsed power'. The CCD clocking will span the bunch train period, with a small overlap for starting before the first bunch crossing and completing readout after the last one. With a duty cycle of only about 0.5%, the power dissipation even at the ladder ends will probably fall below the limits for gas cooling. If necessary, it will of course be possible to supply liquid or evaporative cooling (as was used in NA32 [8]) to the ladder ends, since in these regions the material budget is less critical.

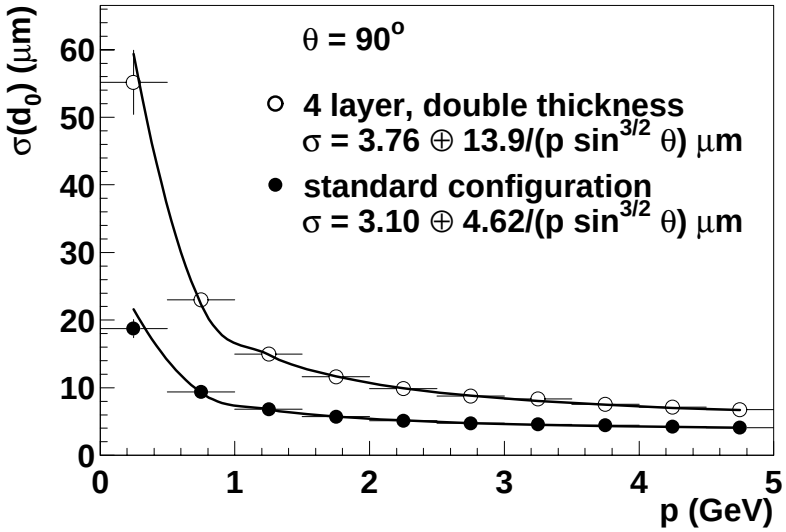


Fig 7: Track impact parameter resolution in $r\phi$ vs momentum for $\theta = 90^{o}$, for 4T solenoid field, and two detector options (see text).

For NLC/JLC, the clocking rates and hence power dissipation can be greatly reduced. This issue has still to be studied in detail, and there is a good deal of flexibility. One option, as for TESLA, will be CPCCDs with bump-bonded readout chips. In this case, the noise level and power dissipation will both probably be minimised by reading out slowly, filling the available 8 ms between trains. Alternatively, a more conventional architecture with a standard multiple output CCD having 10-20 short linear registers, wire-bonded to a local readout chip, may be preferred, particularly if there are significant problems with the bump bonding. But also in this case, noise and power considerations would suggest taking advantage of most of the time available between trains for readout. During the short bunch train, the CCDs will be in a quiescent state, permitting optimal charge collection (mostly by diffusion) in order to maximise the measurement precision.

8 Generic detector performance

In this section, we discuss simulations based on the complete TESLA tracking system, namely the vertex detector, intermediate tracking detector (ITC) and main tracking detector (TPC) operating in a 4T solenoid field. Details of these studies were reported in [2].

One figure of merit for any pixel-based vertex detector can be expressed by the precision with which one measures the track impact parameter to the IP, separately in the $r\phi$ and rz projections. For a set of cylindrical detectors, this resolution can be expressed as

$$\sigma = \sqrt{a^2 + \left(\frac{b}{p \sin^{\frac{3}{2}} \theta} \right)^2}$$

The constant a depends on the point resolution and geometrical stability of the detectors and b represents the resolution degradation due to multiple scattering, which varies with track momentum p and polar angle θ. For the present detector design, the values of a and b are similar for both projections, and take the values 3.1 μm and 4.6 μm respectively. An example is plotted in Fig 7 for the 'standard' vertex detector, and for a conservative design in which the inner layer is removed, the beam-pipe radius is doubled, and the detector layer thickness is doubled. The plot shows graphically the importance of pushing the design to the limits, for any physics which depends on accurate

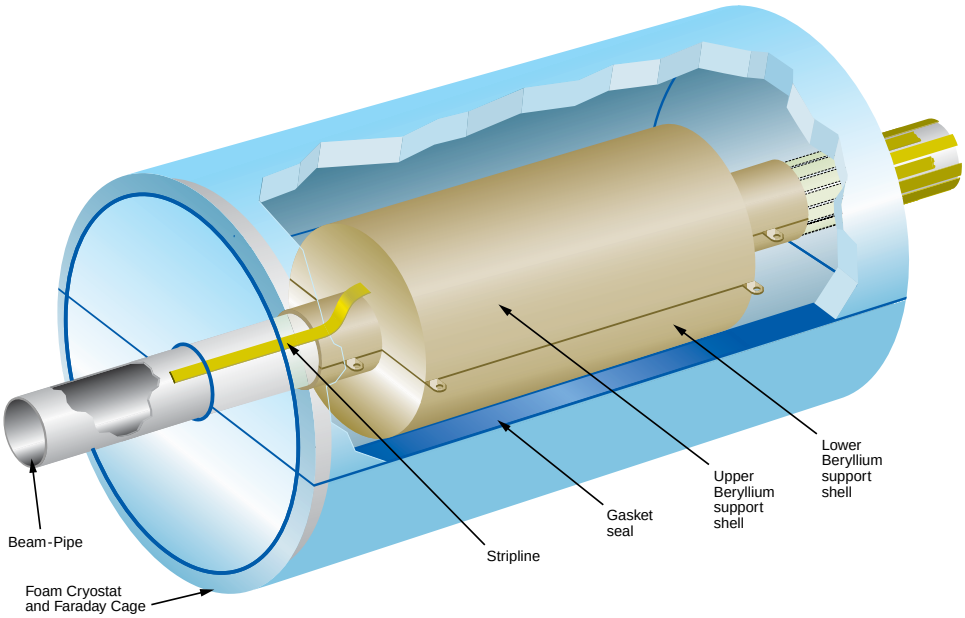


Fig 8: Isometric view of the detector, showing the support shell linking the robust outer sections of beam-pipe.

measurement of low momentum tracks, examples being the measurement of vertex charge or the charge dipole. These calculations are based on a full GEANT description of the TESLA detector, and use the BRAHMS detector simulation program.

The other important performance parameter is the 2-track resolution, which is particularly relevant to the core of high energy jets where the particles traverse the inner VTX layer. With a clean 2-track resolution in space of about 40 μm , CCDs are relatively robust. However, some *B*s decay close to or beyond layer 1, so there are inevitably complex examples. Experience from NA32 shows that these long-lived particles will form a particularly clean category, given unambiguous information from the outer layers. However, these questions need detailed study.

Very similar results have been demonstrated for the NLC/JLC detector. The impact parameter resolution is relatively independent of the outer tracking system, whose main function is to make precise measurements of momentum for each track in the event. In addition, having two independent tracking systems (vertex and outer tracker) will be extremely valuable in debugging the reconstruction code of each separately.

9 R&D programme

The proposed detector with 799 Mpixels is a reasonable evolution from the successful SLD vertex detector of 307 Mpixels which operated reliably for several years in hostile background conditions. However there are challenges which push the design well beyond the performance required for SLD. R&D for the mechanical and thermal design is discussed in Section 9.1, that for the novel CCD architecture in Section 9.2, with the associated readout IC in Section 9.3, and the driver IC in Section 9.4. The issue of radiation effects is discussed briefly in Section 9.5.

9.1 Mechanical and thermal design

Given that there are many good reasons for not wanting to enclose the vertex detector within the machine vacuum, the first material encountered by particles, which degrades the measurement of their impact parameters, is the beam-pipe. For the SLD upgrade detector, a beam-pipe of wall thickness

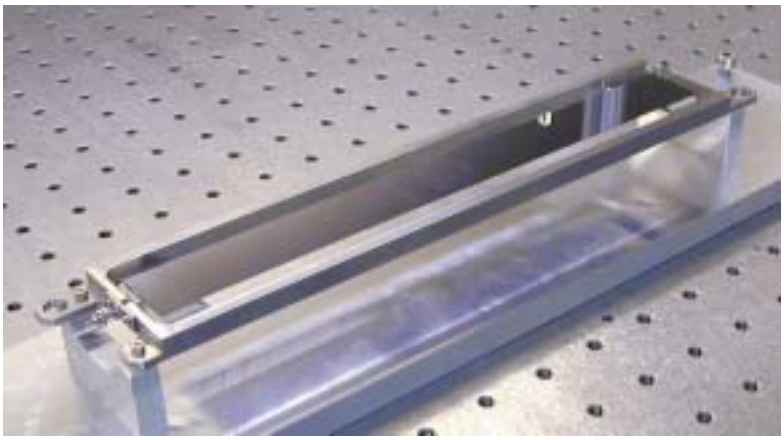


Fig 9: Unsupported ladder (tensioned) made with unprocessed silicon. Overall length 25 cm (two dies butted together and bonded with a thin silicon bridge)

0.75 mm was used. This had a large safety factor with respect to the atmospheric pressure. The main risk was cracking at the braze joints during installation on the beam-line. For the TESLA detector, it is proposed to stabilise the delicate inner section of beam-pipe by means of a rigid clamp at $Z = \pm 15$ cm in the form of the two halves of the VTX support structure, as shown in Fig 8. This sturdy beryllium shell can be made with 1.5-2 mm wall thickness ($\leq$ 0.6% X_0) with no degradation to the tracking performance, since it lies beyond the system used to measure the impact parameter. By following this approach it may be possible to reduce the wall thickness of inner beam-pipe (a cylinder of length 12 cm) to 0.25 mm. However, this needs to be established with test structures, the main concern being stresses on the thick/thin braze joints during installation.

Given the approximately hermetic support shell, the gas cooling can be achieved by axial flow, feeding in at one endplate and out through holes in the other. More robust cooling of the driver and readout chips can if necessary be carried out with evaporative cooling of nitrogen. While there is experience with these techniques in earlier detectors [7, 8] there are new aspects for the TESLA implementation which will require R&D. Minimising the external plumbing needed for the delivery and exhaust of the coolant requires some development; some improvements with respect to the rather satisfactory SLD system can be envisaged.

The construction principles of the 64-ladder detector have been described in Section 6. As with SLD, the detector would be surveyed optically during assembly, layer by layer. Unlike in SLD, due to the opaque support shell, the order of survey would be reversed, starting with layer 5, and would be carried out on each half-detector separately. As usual, the fine tuning of the geometry would be done by track fitting. Achieving systematic errors on a system of length 250,000 microns and diameter 120,000 microns which does not add significantly to the intrinsic precision of ~ 3 microns will be even more challenging than with the somewhat smaller (length 16 cm) SLD detector. The principle of construction based on ladder/annulus blocks fixed at one end and sliding at the other is a proven method of allowing for the otherwise massive effects of differential contraction between the ladders (all operating at slightly different temperatures) and the support shell (which will be slightly cooler at the bottom than the top).

Our most ambitious ladder design concept is that of ‘unsupported silicon’. The idea is to take bare back-thinned CCDs (thickness around 50 microns) and achieve good mechanical stability by (as in SLD) bonding them to ‘ladder blocks’ fixed at one end, sliding at the other, but with the added feature of a small tensioning spring at the sliding end. Test structures of this design have been constructed, as shown in Fig 9. In fact, tests of this ladder showed excellent mechanical stability. For a spring tension in excess of 150 g, the ladder could be pushed at the sliding end so that it sagged visibly, then

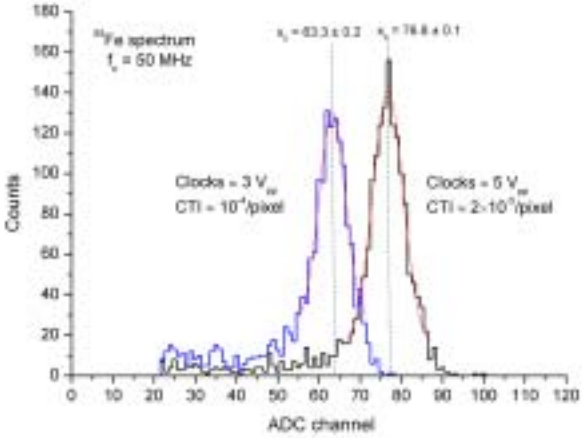


Fig 10: Fe-55 spectra obtained with CCD58 at 50 MHz serial clock rate. The CCD demonstrates good performance with drive clock amplitudes of 3 V_{pp}.

allowed to spring back, and the resulting stability on the sagitta was found to be better than 3 microns. However, while these most encouraging results were being obtained, a separate line of investigation revealed an unwelcome problem. The first results had been obtained with unprocessed silicon. Processed CCDs are mechanically more complex for two reasons. Firstly, the front-side processing (layers of oxide, nitride, metal, polysilicon, etc, some deposited at high temperature), leads to considerable internal stresses. Furthermore, the backside thinning, depending on the process details (lapping, etching, ...) can lead to additional stresses on that side of the wafer. The combined effects lead to considerable curvature (convex or concave, depending on the details of the processed, thinned CCDs). Thus the concept of stabilising a ladder by tensioning is not so simple as stabilising a wire in a wire chamber. Tensioning stabilises the longitudinal profile very effectively, but does not handle cleanly the inevitable transverse stresses. Considerable and rather unstable transverse curvature, varying uncontrollably along the length of a ladder constructed in this way, seems to be likely. Incidentally, internal stresses in back-thinned wafers are notoriously much worse in MAPS devices than in CCDs, due to the more heavily processed front surfaces (more metal layers, etc).

While not yet abandoning the unsupported ladder concept, we are currently more optimistic about what we call the semi-supported option, which is a variant of the SLD ladder design. The mechanical substrate will consist of thin beryllium sheets (possibly 0.25 mm) and the CCDs will be thinned to about 50 microns. The assemblies will be bonded with pads of silicone elastomer as in SLD, to minimise the thermal stresses on cooldown. The idea is to stabilise the ladders longitudinally with springs (as for the unsupported case) and transversely by the rigidity of the beryllium. This concept has the advantage that a ladder becomes a self-supporting item that can be handled conventionally. This is extremely desirable when one considers in detail the procedures for bump-bonding and general assembly. Simulations based on ALGOR and ANSYS are most encouraging, and the first prototype with this design concept has just been made. It looks excellent, but so far has been operated only at room temperature. Cooling studies are about to begin.

9.2 Column-parallel CCDs

A column-parallel CCD is a device in which the serial register is eliminated and each column of the parallel register has its own output stage. Transferring signal charges from the imaging area in parallel allows one to shorten the readout time of the device by 2-3 orders of magnitude. The idea is in principle simpler than the ‘standard’ CCD, however a range of issues has to solved before it becomes a viable concept. One of the particularly challenging requirements for TESLA is the ability to clock the parallel register at up to 50 MHz for the layer 1 CCDs. The impedance of the parallel register is dominated by its large capacitance and the first task must be to reduce the resistance of the

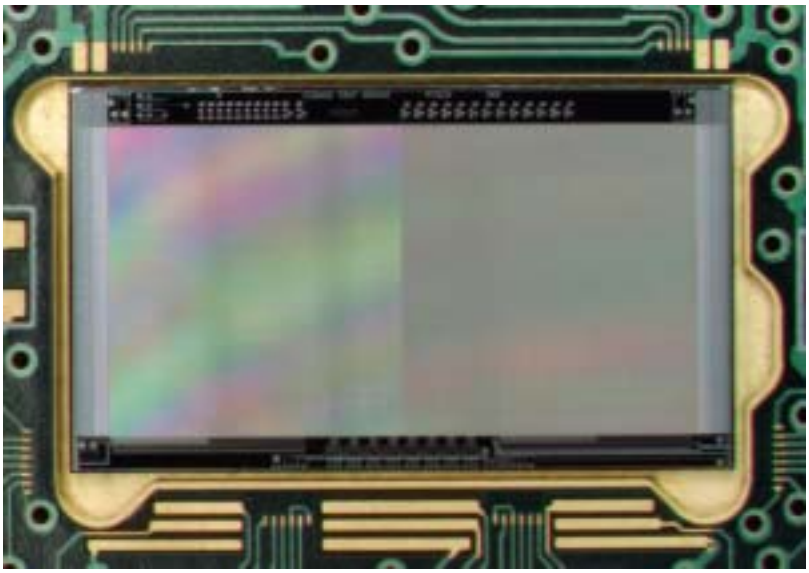


Fig 11: Photograph of the CPC-1 chip positioned in the well of its motherboard. Active imaging region is 15 mm (750 columns) in width.

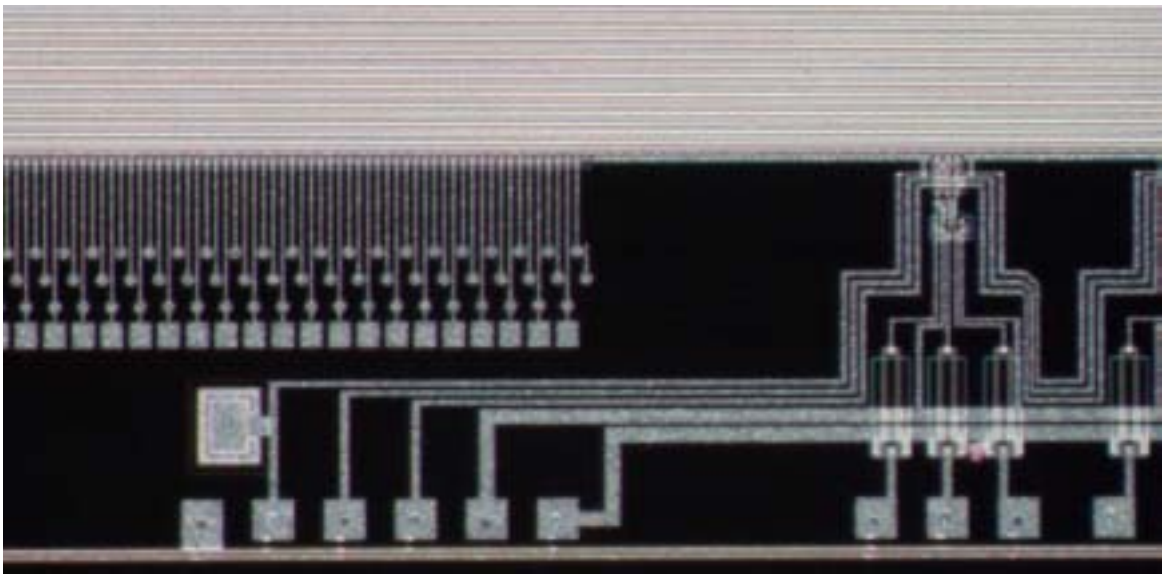
buslines that run along the CCD edge and of the gates that distribute the clock pulses to the interior of the device area.

For technological reasons gates are usually made of polysilicon and have significant resistance, which limits the maximum parallel clock frequency of a typical CCD to only a few MHz. The CCDs for particle detection are not required to be transparent to visible light, which opens the possibility of providing thin aluminium strips (about 5 μm wide) deposited on top of the polysilicon gates in the imaging area, vastly reducing the gate resistance and ensuring efficient propagation of the clock signals over the full imaging area of the device.

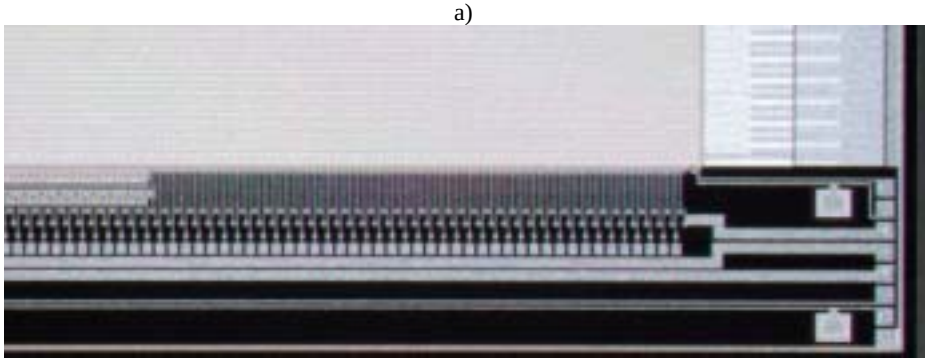
The clock buslines also have to be optimised for minimum losses and parasitic effects. Their resistance can be reduced in a similar manner by depositing relatively thick aluminium on top of the standard buslines. Considerable attention has to be paid to the parasitic inductances of the gates, buslines and the connections to the external driver. Minimising the resistance of the clock path could result in unwanted resonance caused by the large CCD capacitance and even very small parasitic inductance. The entire CCD drive circuit has been extensively studied by simulations with P-Spice, which demonstrate that good quality clocks can be delivered if all paths are optimised and the design incorporates the advanced features described above.

The most promising CCD architecture will be 2-phase with sinusoidal drive waveforms, since this preserves a perfect balance between the currents flowing in the two phases, minimising clock feedthrough to the sensitive output circuits.

CCDs on the outer layers are each connected electrically at only one end, but the required clocking rates are lower. The power dissipation associated with clocking the overall detector at 'standard' CCD voltages would be excessive, but can be drastically reduced due to two fortunate circumstances. Firstly, the potential wells needed to transfer the small charge packets (signal and background) can be relatively shallow. By careful control of the doping and the shape of implants for 2-phase clocking, it is expected that drive pulse amplitudes in the range 1-3 V will prove sufficient, as already developed for some CCDs in lightweight video cameras. In laboratory experiments we have demonstrated operation of a 3-phase CCD at 50 MHz (Fig 10) with serial clock amplitudes of only 3 V_{pp}, which is very encouraging. Secondly, the CCD clocking, as well as all the dissipative electronics, needs to be operated only during the bunch train (with a short early settling period), giving only ~0.5% duty cycle.



a)



b)

Fig 12: (a) Photograph of an area of the CPC-1 showing direct connections (left) and 2-stage source followers (right); (b) array of single-stage source followers (left) and direct connections (right). Rectangular wire bond pads and circular bump bond pads are clearly visible.

Following these procedures, the average power dissipation in the active volume of the detector with 799 Mpixels is calculated to be less than 10 W, easily cooled by a gentle flow of nitrogen gas, as used at SLD.

The readout system for the column parallel CCDs is a subject of an intense R&D programme. The general scheme consists of a readout chip bump-bonded to the CCD, where advantage can be taken of the powerful and dense integrated CMOS electronics on 0.25 μm feature size, which will be further reduced below 0.1 μm during the lifetime of the project. The CCD design team at e2V has been able to lay out single-stage source follower circuits with constant-current first-stage load transistors on a pitch of 20 μm. The external load to be driven (bump-bond connection and preamp input) will be sufficiently small to permit 50 MHz operation with only a single stage source follower on the CCD. Typical source followers on CCDs have relatively high power dissipation and their operating currents have to be carefully selected. Pulsed power will be used to keep the dissipation under control. Furthermore, this circuitry is beyond the edge of the active volume, so more robust cooling systems are acceptable, as discussed in Section 6.

Even more beneficial would be to completely eliminate any transistors on the CCD and connect the output nodes of the device directly to charge amplifiers on the CMOS chip by bump bonds. This would not only further reduce the total power dissipation of the assembly, but would allow continuous reset of the output node with variable time constant. This feature would eliminate the need for a reset pulse and render the detector tolerant of high pixel occupancies, such as may be encountered in

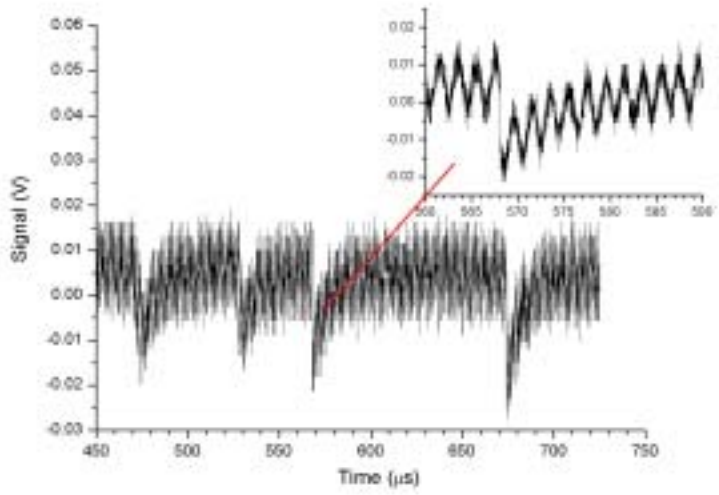


Fig 13: 4 X-ray hits seen in readout of a single column of CPC-1. As seen in the inset, what appears to be noise is mostly a systematic clock feedthrough signal, which is easily subtracted electronically by the technique of correlated double sampling (CDS).

extreme background conditions. This extremely attractive but adventurous possibility will be tested at an early stage in the R&D programme.

Our first CPCCD (CPC-1) was designed by e2V with significant input from the LCFI collaboration and includes many of the features discussed above. It is a 2-phase device with 750(H) × 400(V) 20 μm square pixels. Its production has been completed and several chips have been delivered to RAL for testing.

The CCD has two charge transport regions, clearly seen on Fig 11, and three different output circuits. The area on the left is made with standard 2-phase implants while the other half uses profiled implants which could permit higher clock frequencies at lower amplitudes. The wide clock drive buslines are visible, one pair running along each vertical edge of the device, just outside the imaging area. Connections from the corresponding drive buslines on the motherboard are made by clusters of wire bonds at the top left and right corners of the CCD.

For standalone testing with external discrete electronics the CPC-1 is equipped with 8 triplets of 2-stage source followers, which can drive large external loads (Fig 12(a)).

An array of 125 single-stage source followers with active on-chip loads and 125 direct connections is provided for wire- or bump-bonded connections to the readout chip (Fig 12(b)). The three output circuits are provided for both charge transport sections. Wire-bond connections will be used for initial tests of the output arrays, in which case only one in three outputs can be used. The row of bump-bonds connecting the CCD to the readout chip is staggered to give a minimal pitch of ~40 μm, which complies with available industrial processes. The final stage of testing will be to study the performance of the bump-bonded hybrid assembly consisting of CPC-1 and its readout chip.

The gates in the parallel register of CPC-1 can be metallised to ensure good quality of clocks over the entire area. Special attention has been paid to the buslines, which are widened and can have metal screens to reduce their inductance. Some devices will incorporate these high-speed features as well as a choice of two operating currents for the 1-stage source followers, available as a technological option

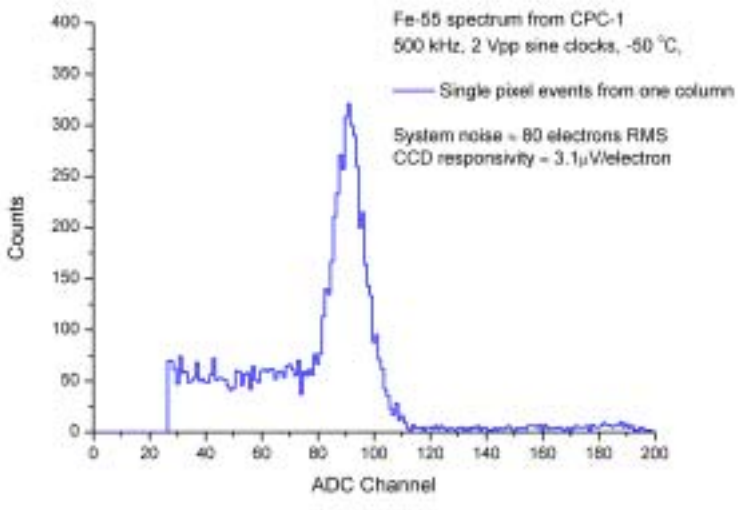


Fig 14: Single pixel events seen in one column of CPC-1 with 2 V peak-peak clocks

in the e2V process. Depending on the results of the first tests, later devices can be delivered with or without those features at no additional cost.

In the case of TESLA, there are various subtle features of the CCD operation, such as the need for fast charge collection into the buried channel, so the epitaxial region will be fully depleted, and the clock phases synchronised accurately with bunch crossings. The Lorentz angle effects from the 4T solenoid field are significant. For these and other reasons, accurate 3-D simulation of the devices under dynamic operating conditions are essential. These studies are now being carried out at two of the collaborating institutes, where the necessary software tools are available.

We have just begun testing our first two-phase column-parallel CCD (CPC-1), with extremely encouraging results. These CCDs lack the structures needed for operation at the highest clocking frequencies, and the initial studies are being carried out at 500 kHz or 1 MHz. Figure 13 shows the trace of a digital oscilloscope observing the output from a single column, where the entire CCD area is being clocked at 500 kHz. To minimise ground currents and capacitive feedthrough, clock drive is provided by anti-phase sine wave pulses. We illuminate the CCD with an ^{55}Fe source, and observe X-rays from the K_α line at 5.9 keV, closely similar in size to the average signals that would be generated by min-I particles traversing 20 μm of active silicon. As shown in the expanded display of one hit, what appears to be noise is in fact clock feedthrough to the output, and is a typical feature of CCD operation. The modest amplitude of the clock feedthrough (comparable to the magnitude of the signal) should be entirely compatible with the preamps on the CMOS readout chips and is most encouraging.

The rms noise observed after passing these signals through a simple CDS filter is around 80 e^-, which is perfectly adequate for efficient min-I particle detection. Initially the data from only one CCD column was available and single pixel events were selected from the X-ray hits. Despite the absence of 2-D information, the single pixel events show a clear peak (Fig. 14), corresponding to an excellent effective node responsivity of 3.1 μV/e^-. The minimum clock amplitude (Fig. 15) at 500 kHz was measured as ≈ 2.0 V (peak-peak), below which the Charge Transfer Efficiency (CTE) rapidly deteriorates. Future devices with non-implanted inter-gate barriers may work at even lower clock amplitudes. Currently we are continuing to study the devices in more detail at much higher clock frequencies.

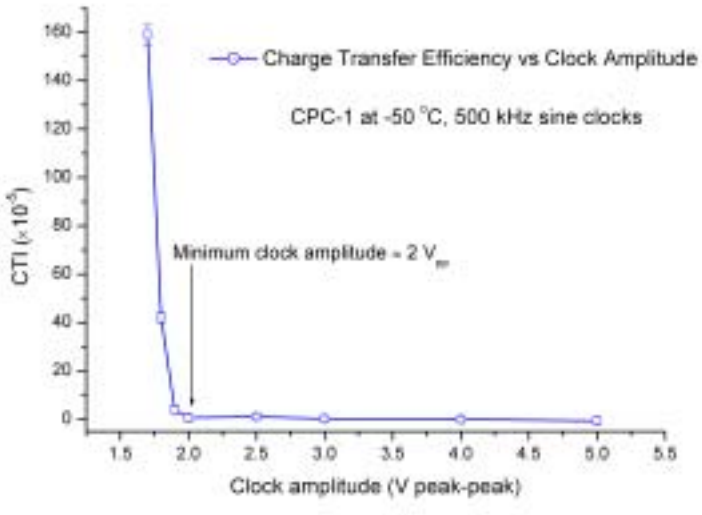


Fig 15: Measured charge transfer inefficiency (CTI) vs amplitude of sinusoidal clocks, operating at 500 KHz

9.3 Readout IC

A team in the Microelectronics Group at RAL has made excellent progress in the readout chip design. A small test chip (CPR-0) with size 2 mm × 6 mm has been designed using a 0.25 μm CMOS process, manufactured and successfully tested. The chip contains arrays of fast 5-bit ADCs laid out on 20 μm pitch, as well as voltage amplifiers designed to accommodate signals from the 1-stage source followers on the CCD. The ADC uses charge-transfer amplifiers in each of its 31 comparators for low power consumption and has shown excellent parameters operating at speeds of up to 50 MHz.

The results from the test chip were used to design the first bump-bondable readout chip CPR-1. It is 6 mm × 6 mm in size and contains 250 ADCs, FIFO, 125 voltage amplifiers and 125 charge amplifiers for the direct connections to CPC-1, one chip on each side of the CCD, with a 5 mm gap in the middle section occupied by the direct-output channels. The ADC outputs are fed into a FIFO array, from which the raw ADC data can be read out serially. The chip has been designed, produced and recently delivered to RAL. After the initial tests to be carried out by its designers, the CPR-1 will be wire-bonded to CPC-1. Although only one in three outputs will be connected, this configuration will provide valuable information on both CCD and readout chip operation as a hybrid module. After these tests are completed, CPC-1 and CPR-1 will be bump-bonded, in which configuration the full capability of the assembly can be realised and evaluated.

The next readout chip CPR-2 (see Fig 16) will include data processing, comprising digital subtraction between successive pixel signals, sensing the signal steps while discarding the empty data on the trailing edge of real signals. These subtracted pixel data are subjected to a pixel threshold set at approximately twice the standard deviation of the readout noise, low enough for full min-I efficiency but too low to be used as the sole means of data sparsification. Signals which satisfy the pixel threshold are used to activate kernel logic which checks the overall signal in any 2×2 cluster around the trigger pixel. All signals above the cluster threshold induce storage in local memory of a defined region (typically 4×6 pixels around the kernel). These sparse data clusters are assembled in a particular format (address, followed by pixel contents in a standard order) and stored in memory. In the full detector, it may be more convenient to implement this memory as a small separate chip mounted on the ladder block adjacent to the readout chip. The design of the next generation readout

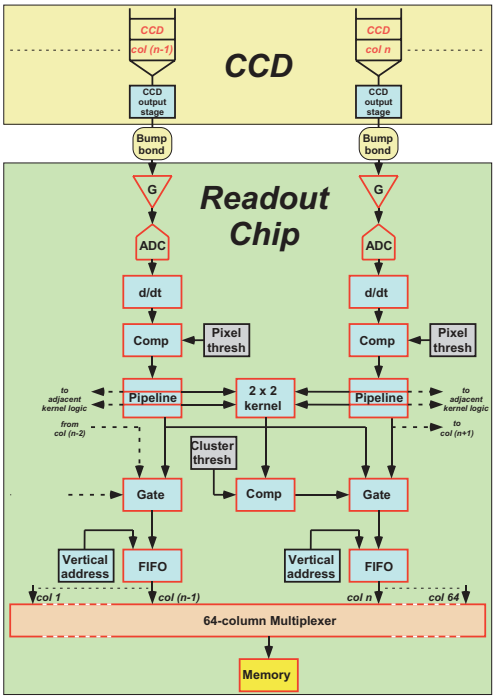


Fig 16: Logic layout of readout IC CPR-2

chip is well underway. Due to the high transistor densities realised with the 0.25 μm CMOS process the increase in chip size needed to accommodate the additional logic is quite modest.

9.4 Driver IC

Design of the driver IC is expected to follow the developments in commercial devices for applications like ADSL drivers, which can deliver high output currents at speeds in the tens of MHz range. The clock driver for CPC-1 will use several miniature ADSL chips which can drive large capacitive load and provide sufficient current capability. It looks possible that the clock driver for the large area CPCCDs can be made of several such chips in a die form. If that turns out to be unsatisfactory, full custom design will be considered.

9.5 Radiation damage effects

Due to the faster clocking and hence more frequent filling of traps, the TESLA detector will be less susceptible to bulk damage than at SLD, where excellent performance was achieved. However, there are still some concerns about neutron damage, which could be serious only if flux levels greatly exceed current expectations. The readout chip could be susceptible to single-event upsets (SEUs) or long-term damage. In any case, the radiation tolerance of modern CCDs with respect to neutrons over a wide range of operating temperatures is not well characterised. The same can be said for the dependence of the radiation-induced Charge Transfer Efficiency (CTE) on the readout speed, where high frequency data is scarce.

One of the essential goals of the LCFI collaboration is to provide a comprehensive study of the radiation effects in the CCDs and readout chips with different device architectures (supplementary channels etc) as a function of temperature. Radiation damage studies were carried out on a high-speed CCD58 irradiated to 30 krad with low energy electrons from a ^{90}Sr source. The CTE was measured in the temperature range from -110°C to -10°C at serial readout frequencies from 1 MHz to 50 MHz. Preliminary results are consistent with the theory of electron capture and emission and indicate that the optimal operating temperature needed to maximise the CTE should increase as the

readout frequency becomes higher. At the moment the results are being compared with simulations and will be published in the near future. Additional tests of a neutron-irradiated CCD58 are planned and will be carried out at Liverpool University.

10 Outlook and route to convergence

As a result of a large amount of imaginative beam optics design work, the LC accelerator scientists are confident that they will be able to deliver a beam-pipe radius of 12-14 mm at the IP, which presents an excellent opportunity for heavy flavour physics. The detector physicists have responded by sketching various pixel-based designs which (if realised) will provide all the tools needed for the highest quality vertex detection in the TeV regime. An intensive period of R&D is now being actively pursued in order to see which of these ideas can be turned into reality.

For the CCD option, the thinking has been based mostly on the SLD experience. However, the first SLD vertex detector required 6 years of R&D, and the challenges for the future LC are at least as great. The LCFI collaboration was funded for a startup R&D programme in 1998. Progress during the early years made it possible to define a detailed R&D programme, aiming to establish the feasibility of the detector concept, with a few fully working ladders. With good luck, this could be achieved over a period of 4 years. However there are bound to be setbacks, and a 6-year R&D period (as for SLD) would appear to be more realistic. The LCFI collaboration was approved in summer 2002 for a full R&D programme based on customised CPCCDs and readout chips. On the basis of progress made in the first year, the estimated overall timescale of 4-6 years to complete this R&D programme appears to be reasonable.

Other pixel-based options for the TESLA vertex detector are being pursued in parallel by other groups, notably CMOS pixels, DEPFET pixels, an SOI-based concept, and hybrid pixel systems. As well as this healthy and important competition, the boundary conditions will only be clearly defined when the world community decides which LC option to build. The vertex detector development work now underway for the CCD and other pixel-based options is generic, though the challenges are quite different between TESLA and JLC/NLC. Even if one knew which accelerator option would be chosen, it would certainly be naive to expect one vertex detector technology to prove ‘the winner’, and an even bigger mistake to predict which that will be. There are many unknown factors. For example, due to some glitch in the R&D programme, the potentially highest performance option could be delayed. In this case, the second-choice option could be implemented for the first phase of the physics programme. For this and other reasons, the need for access to the inner detector region has been given high priority in the overall detector design for all LC design options (TESLA, JLC, LC-L and LC-S).

To provide a little guidance to the non-specialists, Fig 17 may be helpful in indicating some options being actively pursued. The ‘ladder’ at the top of the sketch is the physicist’s dream; a pixel array which somehow telepathically communicates its information to the outside world. The light blue area represents active pixels. Below that, one sees the CCD option. For the current CPCCD design, this consists of pretty much the ideal (only active pixels) over the full fiducial area, plus the readout chips (red) deliberately located beyond this most important area. One MAPS option, FAPS, described in [10] and shown in the next sketch, also places most of the subsidiary electronics beyond the fiducial volume. In this case the electronics is monolithic, ie part of the same wafer, so is shown as dark blue. A second MAPS option [12], shown as MAPS(2) turns the rows and columns through 90 degrees, and so has a considerable amount of subsidiary electronics inside the fiducial volume. This is less desirable, but could prove to be necessary. The DEPFET option ([11] and fifth sketch) needs subsidiary electronics along one edge as well as at the ends. The edge-logic (wire- or bump-bonded) is also undesirable (placing material where one most wants to avoid it) but may be unavoidable for this option. Finally (sixth sketch) the HAPS or hybrid pixel option has readout chips bump-bonded to

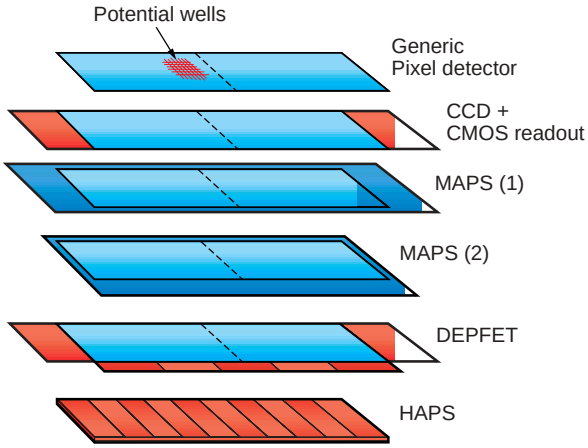


Fig 17: Sketch of different pixel technologies considered for the LC. Blue represents one wafer, and red represents dies from a different wafers, attached by wire- or bump-bonding.

every pixel over the full area of the ladder. This architecture, which also implies relatively large pixels, typically 100 microns square, is by far the worst in terms of material budget. It is the only method conceivable (at present) to survive in the hostile inferno close to the LHC interaction point, but at the LC the much more detector-friendly conditions will permit us to do very much better.

While the R&D programme outlined in Section 9 is focused on the requirements for a vertex detector at the future LC, it is clear from discussions with CCD designers and colleagues in astronomy and SR detection, that the systems being developed will be of great interest to other areas of science and technology. The factor 100-1000 speed increase in CCD readout will be useful to several fields in which time resolved images with visible light or X-rays at high frame-rate are desired. Imaging devices are so pervasive in their applications that technical developments in one area can be guaranteed to spill over into others. Without explicitly engaging in inter-disciplinary programmes, the communication channels provided by the teams of industrial engineers and physicists who design the specialised CCDs for the scientific community have a long and impressive track record for transferring ideas between their numerous application areas. These informal communication channels have over many years been far more effective than ‘specially promoted programmes’ and other short-term initiatives from governments and scientific funding agencies. If the CPCCD design concept proves successful in the first LCFI prototypes, one can expect to see these devices emerging in numerous X-ray and other scientific imaging systems in which much faster readout would be advantageous.

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