LC-DET-2001-059 TESLA
Fev. 2001

Silicon diode, readout and front-end electronics on the proposed W-Si electromagnetic calorimeter

A.Karar
LPNHE-Ecole Polytechnique

Ch. de la Taille
LAL-Orsay

Abstract

Silicon diode, readout and front-end electronics on the proposed W-Si electromagnetic calorimeter are described, after a first pre-study.

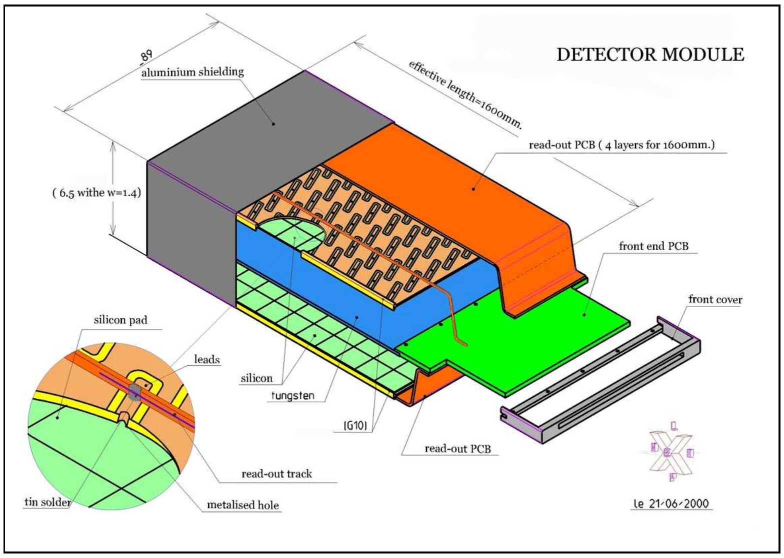

Figure 1: The schematic view of the detector slab, with the read-out lines.

1 The Active W-Si layers

Figure 1 shows a schematic view of the overall Active W-Si layers (detector slab). The Si wafer are located on both side of the tungsten sheet.

To extract the signal, the solution under study for the micro-mechanics of the silicon sensors, is the following: A G10 plane, with metallized holes, is connected to the wires by bonding on the wires side. On the diodes side, a conducting glue is used to connect the metallized hole to the diode, through the amorphous Silicon layer, deposited on the Al sheet, which covers the top side of the diodes (see next section) Between each Si wafer, a dead zone occupied by a guard ring, is also used for a mini-spacer, to ensure the mechanical stability between the tungsten slab and the G10 layers.

1.1 The Silicon PIN Diode

The PIN Si diode for the ECAL have the following charateristics:

- a thickness of 500 μm
- an area of 1 cm^2
- a capacitance of 25 pF
- a leakage current smaller than 30 nA (at 25^0 C)

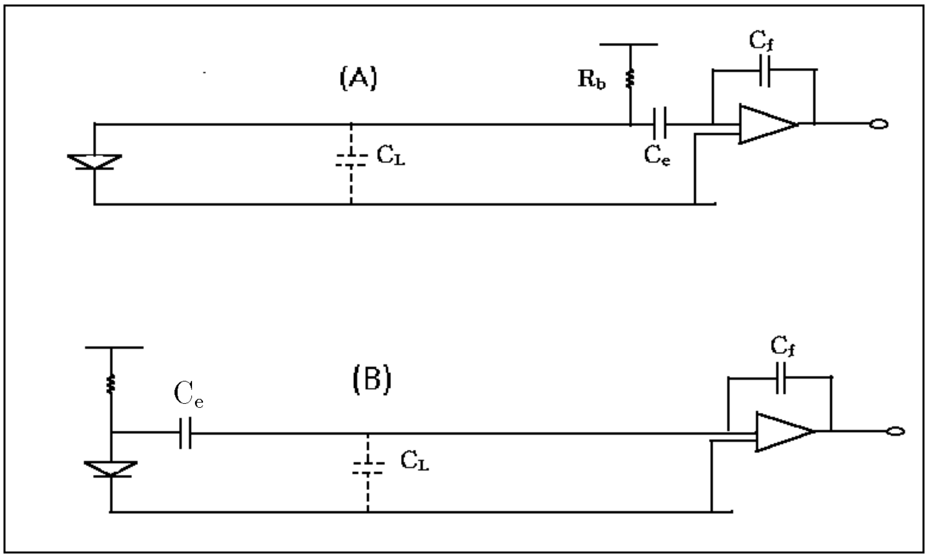

Figure 2: The two possibles solutions for the coupling capacitance and resistance.

- a polarisation voltage larger than 100 V

Hereafter, we will use a Si wafer of 3x3 diodes as an example. As the diodes are at variable distance to the front-end, from few centimeters to 1.6 meter, each pad is connected to the front-end by a wire, while the back side of the diode is connected to the tungsten slab, acting as a return path.

From such a design, we will discuss now the diode polarisation, more precisely the AC coupling, in which the leakage current is not transmitted to the pre-amplifier level.

Figure 2 shows the schematic view, with the two possible locations for the coupling capacitance and resistance. [1] As the blocking capacitor C_e cannot be made larger than 1 nF, it is better to place the capacitor close to the diode so that the collected charge does not depend on the wire capacitance (up to 100 pF). This is confirmed by simulation as shown in figure 3. The solution (B) can be made by a direct deposition, on the PIN Si diode, of a thin layer of amorphous silicon. The capacitance will be made of amorphous silicon nitride (a-Si-N). In order to keep the isolation we need a thickness of 3 μm, which leads to a capacitance of 1 nF for an area of 0.5 cm^2. For the resistance, a small layer of amorphous Silicon at high resistivity, easy to obtain with this technology, would do it. In one Si wafer, all these resistances will be connected to each other, and to the bias line.

Figure 4 describes the proposed solution, while figure 5 shows the arrangement of the silicon wafer, here in a case of 3x3 diode wafer. An important point has to be noted: this

[1] A DC coupled solution (with the preamp. as a virtual ground for the return currents have been rejected as a a short circuit on one diode would bring the HV for the whole barette down

type of direct amorphous silicon deposition, also helps for the fragility of the PIN diode, and would allow to use easy and low cost bonding between diode and the wire of the read-out line.

A prototype corresponding to the solution proposed here, is under study, in collaboration with the PICM-Ecole Polytechnique laboratory [1], who has a large expertise in these types of technology.

2 Front-end electronics

2.1 Introduction

The front-end electronics of the TESLA calorimeter is extremely demanding in terms of integration : it exceeds by orders of magnitude the compacity of present readout systems of calorimeters. Conversely, the technical requirements are not so stringent : the large dynamic range (15bit) is typical of calorimeter electronics ; the noise should be a few thousand electrons and the speed is about 6 to 14 times less than LHC readout. The front-end electronics is located at the end of the modules in the plane (X,Y), in the interspace between ECAL and HCAL. Each barrete (150 pads) would be read by a front-end chip which would integrate preamps, shapers, local storage, zero suppression and multiplexed data output.

An important feature of the front-end is its local trigger ability on the MIP [2]

This will require to set a threshold around 0.8 MIP and to keep the electronics noise below 1/10 MIP= 4000e- in order not to trigger on the noise. To achieve such low figure, the capacitance on the input (dominated by the stripline) will need to be minimized to less than 100pF and a very low noise preamplifier is mandatory.

As shown in Fig.6, the maximum signal in a cell for a 400 GeV electron is 450 MeV, corresponding to 20 pC The dynamic range is thus 20pC/4000e- = 30000 $\approx$ 15 bits. As usual the precision should be below the constant term of the calorimeter, namely 0.4% = 8 bits.

The machine parameters allow a shaping time of about 150 ns. The more demanding for the point of view of the ouput rate/train is the Bhabha process. It is due to the large Bhabha cross section and more important to their largely biased angular distribution. Taking into account the channel multiplicity and the cross section, Bhabha process at the Z peak is the worst situation. In this case, the number of events per train is about 40, with about 600 channel hits for each electron. At the level of a front-end chip, however, the number is relatively small, with a maximum of 30 channels/train/front-end. Now, taking

[2] With a 500μm depletion depth, the MIP signal is around 40,000e$^-$.

into account the Z production and decay, we have to add about 120 channels/train/front-end. In this first study, the beamstrahlung production is neglected. Therefore, for each front-end chip, a maximum number of 150 channels have to be read out every burst i.e. every 200 ms.

However, the space available for the front-end chip is small, about 2*1*0.4 cm^3. This suggest to house 8 front-end chips on a small PCB which connects to the module. The chip would have order of 200 pins, likely in a μBGA type package. The power dissipation should be kept below 0.5W/chip, giving 3 mW/channel *in average* [3]. Such a power dissipation leads to about 100KW dissipation for the overall calorimeter front-end chips. Thermic calculation suggest that a one inch tube of water is sufficient to cool the system.

2.2 Front-end architecture

The key feature of the front-end is to store only the events over threshold together with their time tag. The architecture shown in figure 7 is mostly based on analog blocks to minimize power dissipation, but it could also be largely digital from the local storage. Once again, although the chip architecture is based mostly on existing blocks, the overall integration and the operation at very low power will need further studies.

2.2.1 Preamplifiers, shaper and discriminator

To minimize the noise at the moderate operating speed, the preamplifiers are of the charge sensitive type. They are connected to the detection pad via a 1m long transmission line for which an accurate impedance matching is not necessary[4]. The maximum signal of 20pC needs a rather large feedback capacitance $C_f \approx 10$ pF in order to be handled linearly, giving for the MIP a signal of 0.6 mV, not straightforward to handle up to the trigger in a mixed analog-digital chip[5].

Keeping the noise below 5000e- will require a noise spectral density $e_n < 2$ nV/$\sqrt{\text{Hz}}$, which corresponds to a transconductance of 5mA/V. In that case, assuming a total input capacitance of 150 pF (pad+line) the series noise would be 3500e-. A negligible parallel noise (500e-) will require a leakage current below 0.5μA. This can be obtained with a PMOS input transistor[6] of W/L=2000/0.6, operated at 0.5mA drain curent. The preamp input capacitance would then be around 30 pF (cf. Fig. 8).

[3] the small duty cycle (1ms/200ms) will certainly allow operation with active and idle mode to save power.

[4] The line impedance will be typically 50-100 Ω, whereas the preamplifier input impedance will be a few hundred ohms, due to the limited power available. The few bounces will not last more than 10-20ns and have negligible impact at slow shaping.

[5] At this stage, a non linear preamplifier or a multigain preamp would be worth further studies.

[6] Compulsory for negligible 1/f noise.

The low power operation will necessitate to split the dynamic range into several gains, to limit the dynamic range to 8-10 bits on each gain. A typical arrangement would be 4 gains (1-4-16-64) of 10 bits [7].

In the same stages of gain, a differentiation and two integrations would be taken in order to optimize the signal to noise ratio. As shown in Fig.8, the noise gets rather flat and a peaking time close to the bunch interval (300ns) would be most convenient. This will allow to activate the subsequent track and holds with the machine clock [8]. In parallel, as set of discriminators would flag which is the correct gain for the data (the largest not saturated). This gain value could be "analogized" for subsequent storage to minimize area and power.

The high gain shaper output is also used to discriminate on the MIP signal. The gain should be large enough (10-20 mV/MIP), not to care about DC levels for the trigger and allow a common threshold around 0.8 MIP for all channels. A fully differential structure is foreseen to alleviate offset and common mode noise problems. In order to have a deadtimeless operation, some local storage will be necessary. As the chip is mostly analog, the data will be stored in a SCA which whould be 10-100 cells deep. For each local trigger, the bunch crossing number would be stored on 2 capacitors, as well as the energy and the gain, requiring 4 capacitors per channel. Its limited dynamic range (8-10bits) makes it relatively straighforward, but its depth remains to be optimized. As mentionned before, this part could be digital if competitive in terms of power dissipation[9]

2.2.2 Readout

There are typically 150 channels to be read every 200 ms, which is a very modest data flow. For each channel, events above 0.5MIP are stored together with the BCID. These events would be serialized onto an

anolog line to the subsequent Read-out-buffers located outside the calorimeter. A possible data format could thus be of 5 analog [10] 10 bits "words" : CH# (8 bits), BCID HI (6 bits) + BCID LO (7bits) + Amplitude (10 bits) + Gain (2 bits).

The output data frequency still needs to be determined[11]. The digital part of the readout (number of cables to ADC's, tokenring, ADC's,...) will studied in a separate note.

[7] The number and values of gains depends on the dynamic range of the following stages and will be optimized upon prototype results.

[8] an adjustable delay would allow to always sample at the peak while tolerating timing dispersions between chips.

[9] In that case, a 10bit ADC would convert the energy and the BCID and gain would be stored digitally.

[10] in this proiposal, the BCID and channel number are analog signals on 8-10 bits, given by a few simple DAC, mostly to save power and reduce the digital on-chip activity. Obviously, they could also be provided digitally if analog performance is not degraded.

[11] Taking the full 200 ms inter-burst is probably power saving but more demanding on the data storage. Outputing at high speed and during short periods alleviates this request but may be more noisy.

2.2.3 Controls and calibration

Handling a multigain front-end with the specified accuracy will request a precise calibration system. The classical charge injection through a precise capacitor is foreseen, with the provision of a trimming system to control the uniformity. Several control features will be necessary and will be implemented on the chip and loaded through a serial line.

2.3 Prototypes and Schedule

A first prototype will be quickly needed in order to check the feasibility of such architecture. The main concerns are the em compatibility between low level analog circuitry and digital signals as well as the accuracy required. A chip could be submitted in 0.35 um CMOS AMS during the summer 2001.

References

[1] Laboratoire : Physique des Interfaces et Couches Minces
http://www.lpicm.polytechnique.fr/

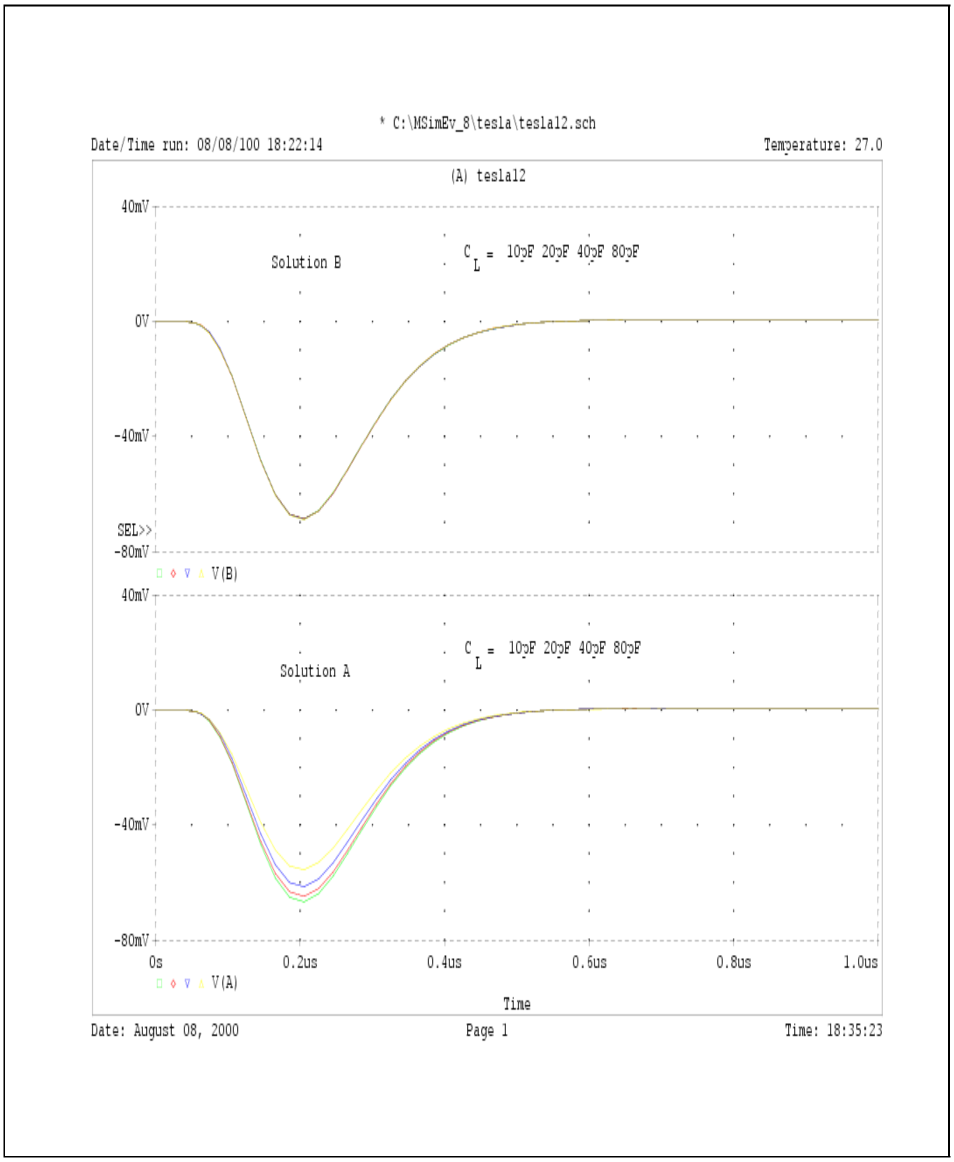

Figure 3: Results of the P-spice simulation.

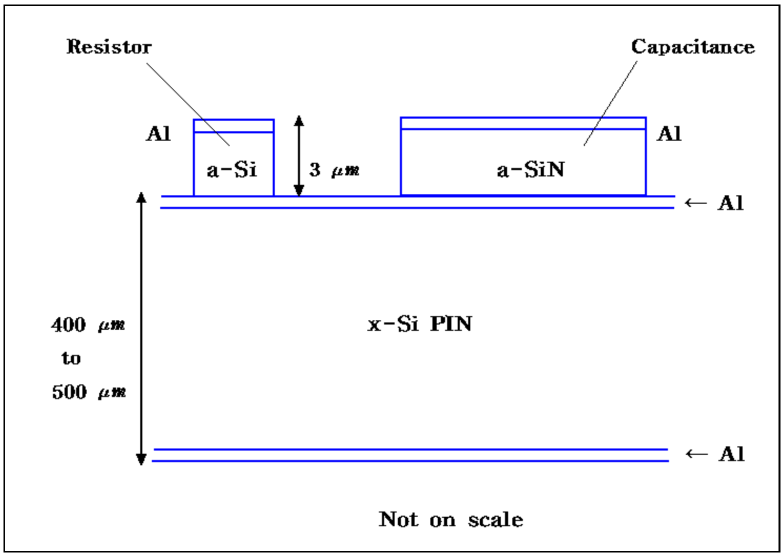

Figure 4: Schematic view of the PIN diode with the amorphous silicon deposited .

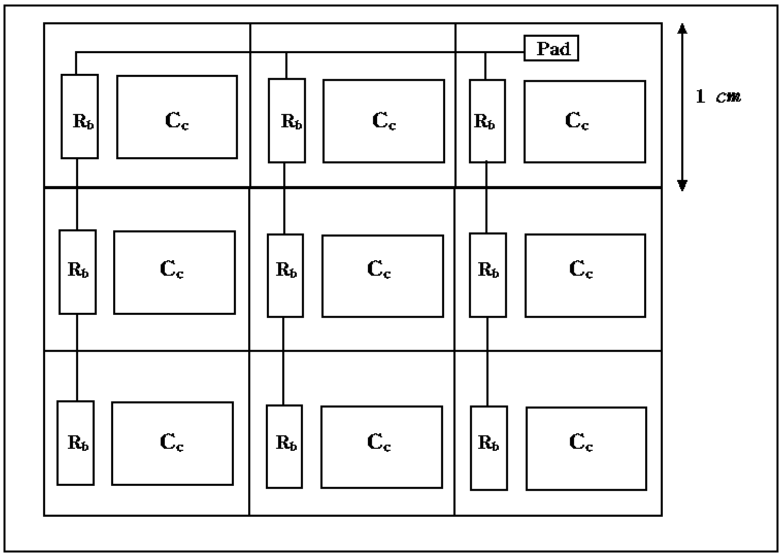

Figure 5: Schematic view of the arrangement of the Silicon wafer, for the case of 3x3 diode wafer.

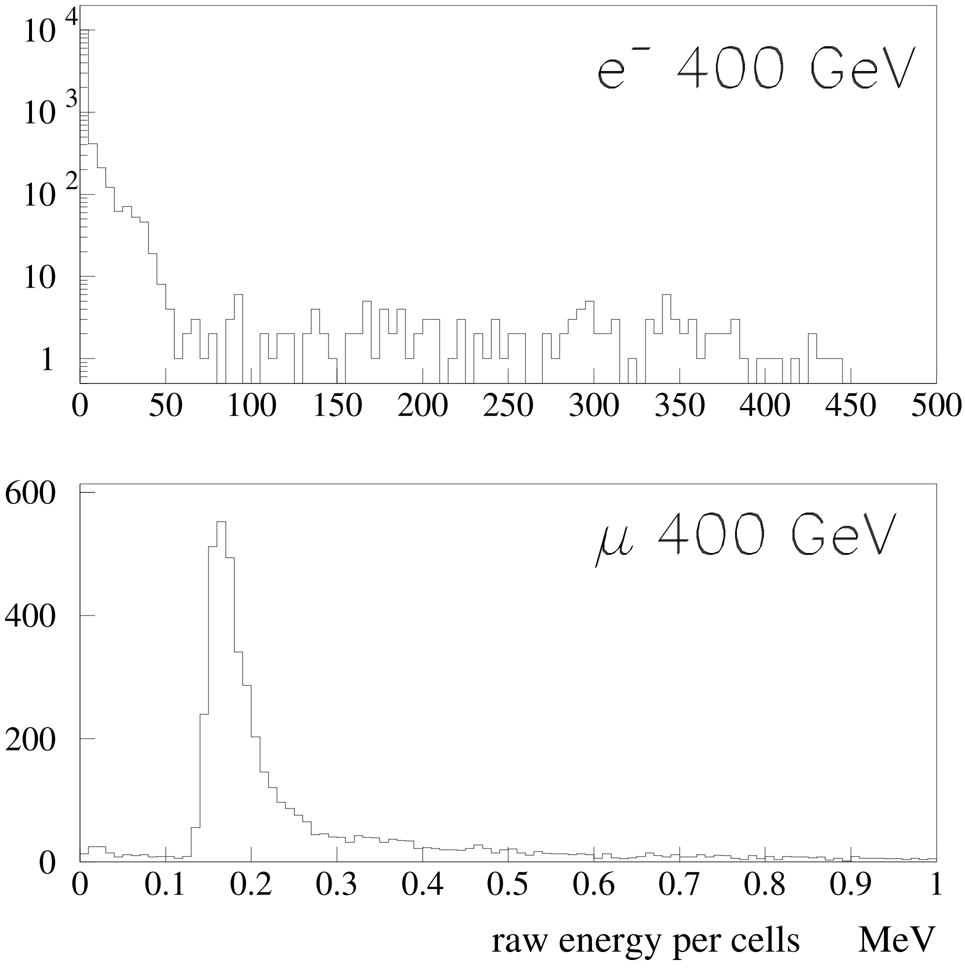

Figure 6: Energy deposited per pad for 400 GeV electron and muon

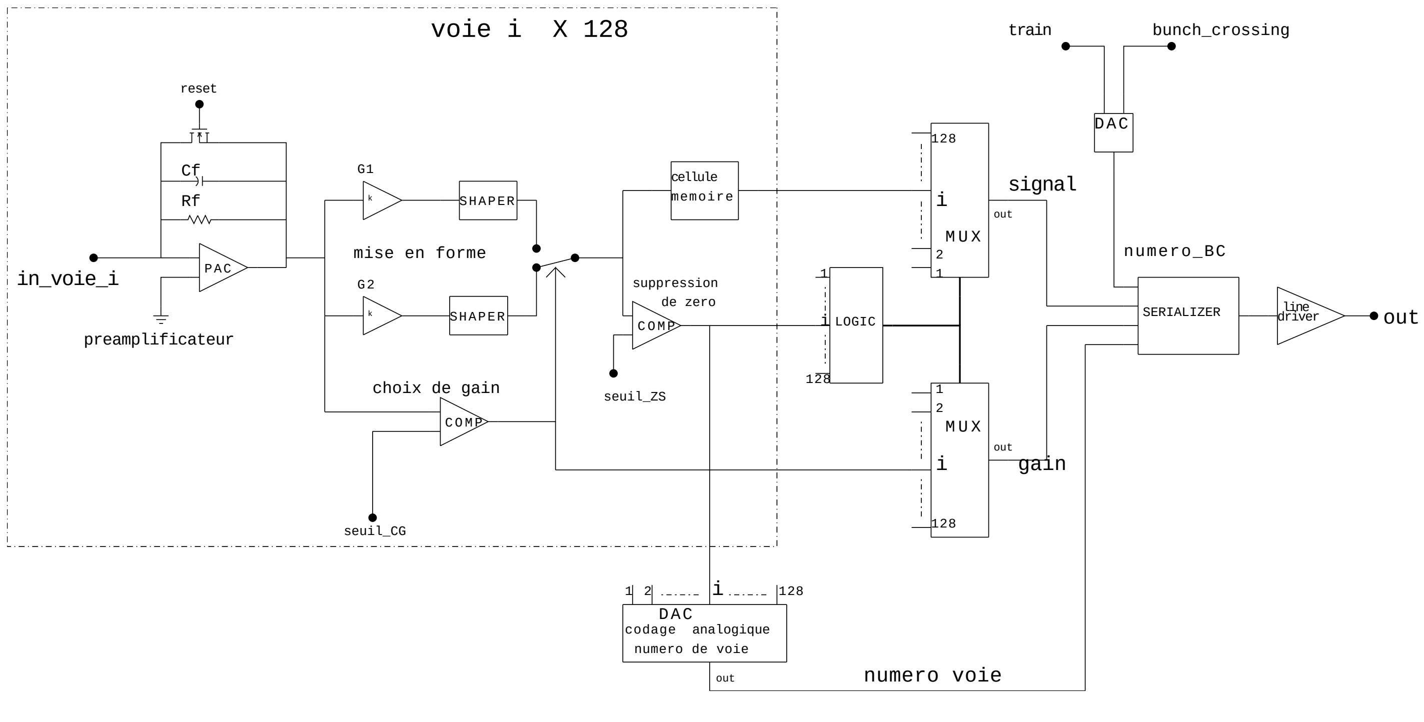

Figure 7: Synoptic diagram of the front-end architecture.

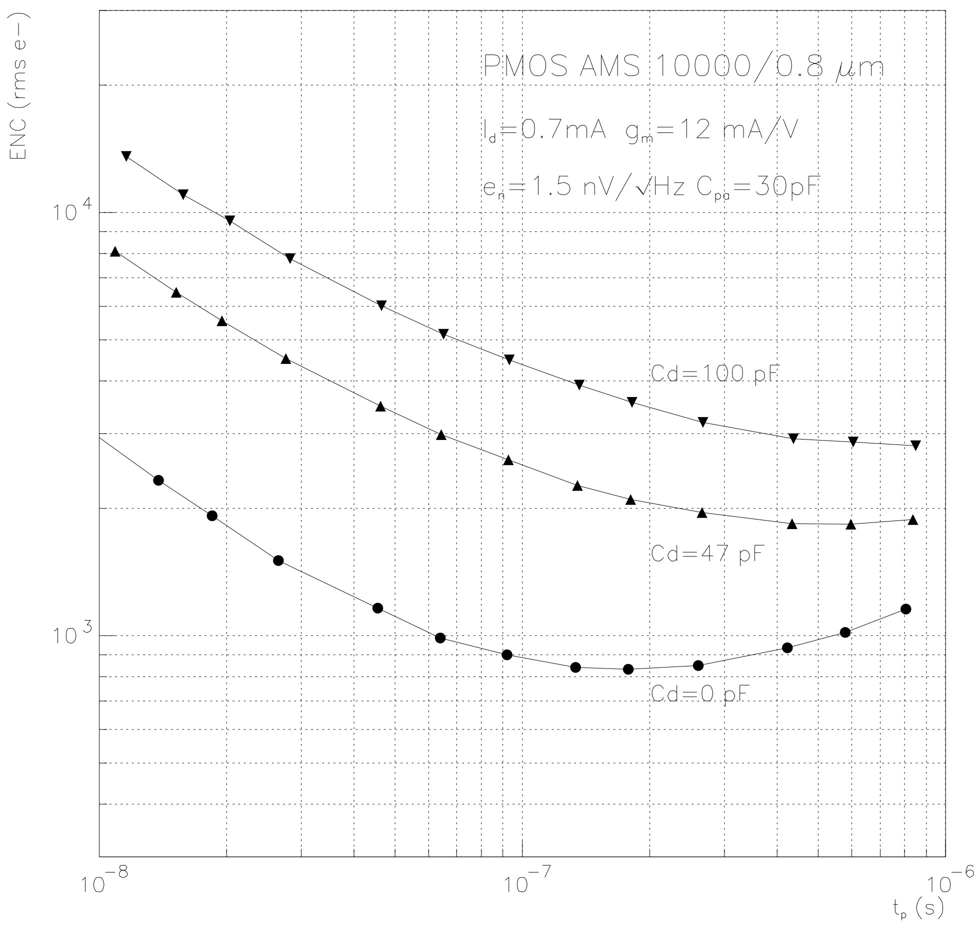

Figure 8: Measured noise performance of a preamplifier similar to the one proposed here, using a 10,000/0.8 μm AMS PMOS input transistor, as a function of the shaping time. Depending on the diodes location, the noise would vary between the two top curves, amounting to 2000-3500 e^{-} at T_p= 200 ns